5890

National® Brand

Narrow Ruled White Paper

Single Subject

Dennison National Company, Holyoke, MA 01041

0 73333 31885 2

31-885

80 Sheets/11 x 8½

5890 Fundamentals

5890 Fundamentals

Overview

Major Components:
- Processors (two stacks)
- MSU
- System Controller (SC)
- External Unit
- IOPs + IHs
- Console Subsystem

CPU Subsystem - Consists of two closely coupled processors, CPU Ø and CPU 2, each containing an I-Unit, E-Unit and cache. Cache consists of a 32K instruction buffer and a 64K operand buffer.

Pipeline: 5 phases -

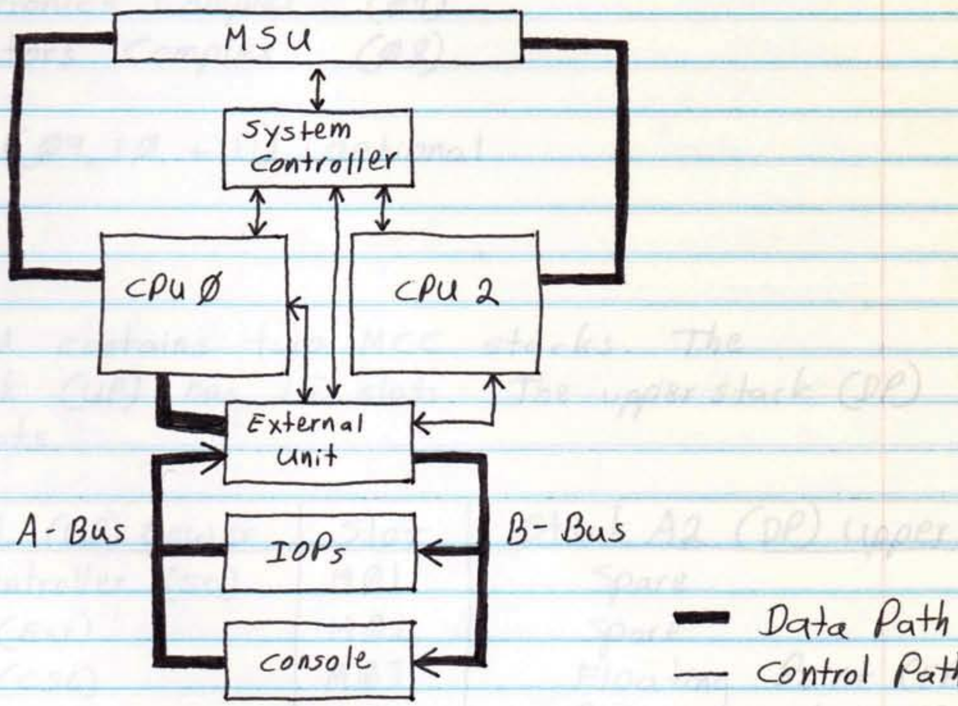
D - Decode Instruction
A - Generate Operand Address
B - Fetch Operands
X - Execute Instruction
W - Write Results

System Controller - Processes all requests for data from storage. These requests may come from either CPU or any IOP. The System controller also ensures data integrity.

MSU - May hold up to 256 megabytes. The System Controller presents requests to the MSU Switchbox. Array cards use 256K chips.

I/O Subsystem - consists of IOPs, IHs, and External Unit. The External Unit processes all I/O instructions. It creates a B-Bus message and passes it to the appropriate IOP (or to the console). When the IOPs or console request data, the External Unit makes the request to the System Controller. Data coming from an IOP moves on the A-Bus to the External Unit.

A 5890 may have up to four IOPs, each supporting 16 channels (via a 16 slot microcoded processor). Up to four channels on each IOP may be configured as byte channels.



Note the data paths to the MSU. All control lines go through the System Controller, but the data path goes to each CPU. CPU Ø also serves as the MSU data path for the External Unit (and thence to the IOPs).

Physical Locations

Mainframe
- MSU (Ø1)
- PRU (Ø2)
- PSU (Ø3)
- SSU (Ø4)
- CEU (Ø5) Optional

PDU (Ø6)

MOC
- Electronics Complex (Ø7)
- Operator's Complex (Ø8)

ROCs (Ø9, 1Ø, + 11) optional

Stacks:

The PRU contains two MCC stacks. The lower stack (UP) has 15 slots. The upper stack (DP) has 13 slots.

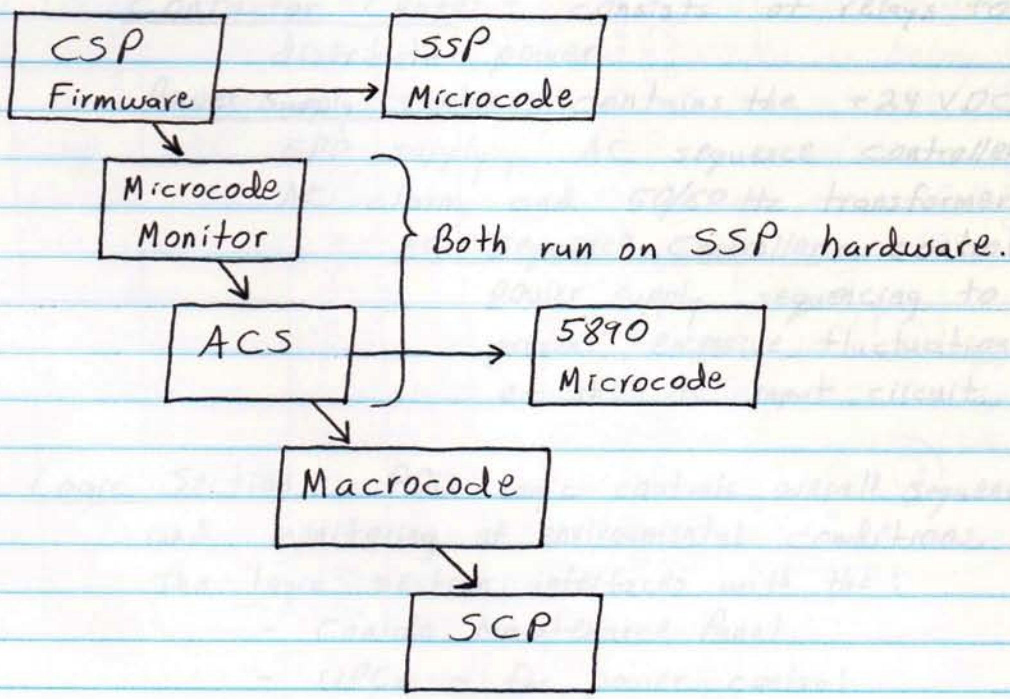
Stack A1 (UP) Lower	Slot	Stack A2 (DP) Upper
System Controller (SC)	MØ1	Spare
External (Ext)	MØ2	Spare
Console (CSL)	MØ3	Floating Point (FP)
IOP Ø	MØ4	Process Control (PC)
IOP 1	MØ5	BUF2
IOP 2	MØ6	Fixed Point (FX)
Basic Error Logic (BEL)	MØ7	Effective Address (EA)
Cache Controller (CC)	MØ8	BUF1
BUF Ø	MØ9	BUF Ø
BUF 1	M1Ø	Cache Control (CC)
Effective Address (EA)	M11	Basic Error Logic (BEL)
Fixed Point (FX)	M12	IOP3
BUF 2	M13	Spare
Process Control (PC)	M14	//////////////////
Floating Point (FP)	M15	

MSU:
- Swing Gate (4 quadrants, 20 array, 5 control, each).
- 6 Power Supplies
- PDB

PSU:
- 19 Power Supplies
- 2 UPCs
- PDB

Console Overview

Initialization Sequence:



Power

Functions of the PDU:

1. Controls power-up and power-down sequences.
2. Supplies DC power to the UPCs.
3. Sequences the UPCs.
4. Distributes AC power (60 Hz + 400 Hz)
5. Monitors for environmental and power problems.

PDU Components:

AC Distribution Section - consists of:

AC Input Center - composed of connectors and circuit breakers for attachement to 60 Hz and 400 Hz sources.

Contactor Center - consists of relays to distribute power.

Power Supply Center - contains the +24 VDC EPO supply, AC sequence controller, AC alarm, and 50/60 Hz transformer.

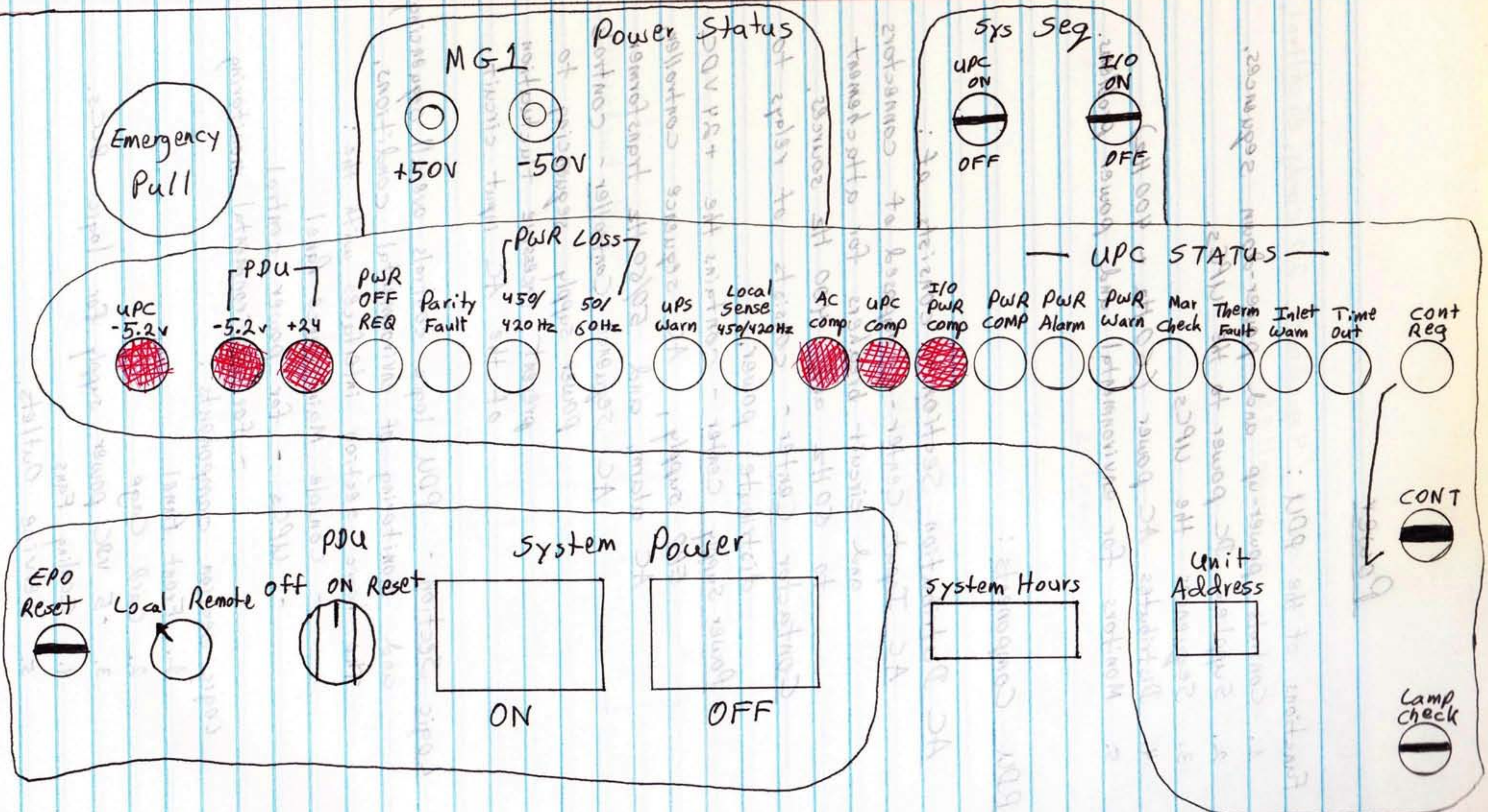
AC Sequence Controller - controls power supply sequencing to prevent excessive fluctuation of the AC input circuit.

Logic Section - PDU logic controls overall sequencing and monitoring of environmental conditions, The logic section interfaces with the:

- Console Maintenance Panel
- UPCs - for power control
  - for environmental monitoring

Logic section components:

1. Front Panel
2. Card Cage
3. -5 VDC power supply for logic BCCs.
4. Cooling Fans
5. Service Outlets.


Emergency Pull
Power Status
MG1
+50V
-50V
Sys Seq.
UPC ON
OFF
I/O ON
OFF
PDU
PWR LOSS
UPC STATUS
UPC -5.2v
-5.2v
+24
PWR OFF REQ
Parity Fault
450/420 Hz
50/60Hz
UPS Warn
Local Sense 450/420Hz
AC comp
UPC Comp
I/O PWR comp
PWR COMP
PWR Alarm
PWR Warn
Mar Check
Therm Fault
Inlet Warn
Time Out
Cont Req
CONT
EPO Reset
Local
Remote
PDU
Off
ON
Reset
System Power
ON
OFF
System Hours
Unit Address
Lamp Check

= Normally On

PDU Panel

EPO - pull switch / manual reset.
Power Status - motor generator +50 V and -50V contacts.
Sys Seq - (System sequence) - Toggle switches control power to the UPCs and I/O.
Indicators:
UPC -5.2 - when on, -5.2 VDC is available for UPCs.
PDU -5.2 V - voltage is available to the PDU.
+24 VDC - on indicates +24 VDC is available to the PDU. Off indicates the +24 supply is off or EPO is thrown. EPO Reset activates EPO circuits.
PWR OFF REQ - Power Off button has been pressed.
Parity Fault - PDU logic has detected an error in PDU ROM.
PWR LOSS - indicates if either 60 Hz or 400 Hz has dropped below minimum voltages.
UPS WARN - UPS has switched to back-up power source.
Local Sense 400/420 Hz - if on, 400 Hz is being sensed at the source, rather than at the PDU.
AC Comp - AC power-on sequence is complete.
UPC Comp - All UPCs have powered up successfully.
I/O Pwr Comp - I/O power sequence is complete.
UPC status
PWR Comp - all frames have powered up.
PWR Alarm - an alarm was detected. See Unit Address.
PWR Warn - non-fatal power problem was detected.
Margin CHK - a bus is in margin. See Unit Address.
Therm Fault - a UPC has detected a thermal alarm or warning.
Inlet Warn - underfloor air is too warm.
Time Out - If a UPC fails to send UPC complete within 7 seconds, sequencing stops.
Cont Req - resumes power sequencing.
EPO Reset - resets the +24 VDC contactor.
Local/Remote -
PDU ON/OFF/Reset - controls the -5.2 VDC supply for PDU logic. Reset reinitializes PDU logic but maintains power to the system.
System Power ON/OFF - ON is red while sequencing on or off.
Unit Address - hex identifier of UPC reporting problem.

PDU Logic cards:

Slot	Function
2	ROM
4	Control (microprocessor)
6	Test card
8	PDU-MOC interface
9	UPC interface
15, 16, 17	Peripheral interface
23	Front panel interface
25	Console interface
28	AC interface

UPC power comes from a -5.2 VDC supply in the PSU frame and is distributed through the PDU.

Power Supply Unit (PSU) - frame Ø3 - contains 19 power supplies, provides and monitors power to the PRU, monitors console logic gate power, and powers the system oscillator (in the SSU).

Power Distribution Boxes (PDB) - are located in the PSU, MSU, and PRU. All cabling from the PDU arrives at a PDB.

Unit Power Controllers (UPC) - Two are in the PSU and one is in the SSU. The UPC
- monitors power supplies
- monitors temperature and airflow
- sequences DC power

The upper UPC in the PSU controls the lower CPU stack, the console, and the system oscillator. It controls 12 power supplies.

The lower UPC in the PSU controls the upper CPU stack. It controls 8 power supplies.

The UPC in the SSU controls any CCAs and the MSU power supplies. It controls 14 supplies.

Each UPC panel has three sectrons:

Power Sequence - contains the local/Remote switch and thumb-wheels to manually sequence the supplies.

Power Supply Status - contains a LED for each power supply plus alarm indicators (UV, OV, and OT). When a power supply has a problem, its LED goes out.

Environmental Status - reports airflow and temperature alarms and warnings.

The UPCs will shut off power when:

- Reduction in airflow
- Increase in temperature
- DC bus voltage deviates from nominal.

Each UPC has five BLCs

Power Supplies

All CPU power buses have redundant supplies. Power supplies cannot be repaired when they fail. They must be replaced.

Locations:

- PSU - 19 Supplies
- MSU - 6 Supplies
- SSU - 10 Supplies

Types:

Quantity	Description
27	Type 15 Switcher, 300 A, -2, -3.6, -5.2, +5, + +5.7
3	Type 10 SCR, 125A, -2, -3.6, -5.2, +5, + +5.7
2	+24 VDC (PDU + MOC Only)

The voltage produced by a given supply is governed by jumpers in the cable connector.

Environmental Sensors - 3 types:

- Airflow
- Thermal
- Fan - the LSI stacks and the power supplies in the PSU have RPM sensors to detect cooling fan failures.

Power Control

To power-up from the MOC:

1. Ensure that 400 Hz and 60 Hz are available.
2. Place all panels in REMOTE.
3. Toggle EPO Reset at PDU.
4. Press SYSTEM POWER ON at the MOC.
   PDU SEQ should go on indicating sequence is in process. When it goes out, the 5890 is powered up.

To power-up from the PDU:

1. Ensure that 400 Hz and 60 Hz are available.
2. Place all UPCs in REMOTE.
3. Set the PDU to LOCAL.
4. Toggle EPO RESET.
5. Press POWER ON.
6. Set the PDU to REMOTE.

Troubleshooting:

An alarm indicates a severe problem and will cause the system to power-down.

A warning indicates a non-fatal error. For example, if a redundant power supply fails, a warning will be issued. This will be indicated at the PDU, UPC, and in response to the ACS command:

Q STAT PCM

Power FRUs:

- Power Supply
- Fans
- Cables (not likely)
- UPC controller board

For diagnosis, use the 5890 SMAPs in the Power Manual.

NEVER turn off a UPC while it is in REMOTE mode. This can destroy the controller BCC.

Even when the system is powered-down, the 60 Hz circuit is still alive. The PDU has a circuit breaker for each power supply.

- CPU -

Scan Facility

Pages	Function
Ø - 99	General Information
100 - 199	I-Unit
200 - 299	E-Unit
300 - 399	CPU Storage
103	Error history latches - the contents freeze upon error detection.

The CPU Subsystem has three components:
- I-Unit - coordinates all CPU activity.
- E-Unit
- CPU Storage

I-Unit functions:
1. Instruction Fetch
2. Operand Fetch
3. Execution (passing to E-unit)
4. Handle interrupts
5. Provide Timing facilities

I-Unit logic lives on three MCCs:

MCC	Upper Slot	Lower Slot
PC	4	14
EA	7	11
CC	10	8

Microcode for I-Unit operation is stored on all three MCCs.

I-Fetch

Instruction fetching is an asynchronous process (subject to interlocks) which keeps the five-phase pipeline supplied. The Instruction Word Register (IWR) holds six half words of instructions.

The Pipeline

Phase	Function
D	Decode - instruction is taken from IWR and decoded.
A	Effective Address Generation of the operand.
B	Fetch Operand - operand is requested, and if available, read.
X	Execution is performed by the E-Unit.
W	Write - results are placed in registers or storage.

Each phase of the pipe ordinarily takes one machine cycle. Up two five instructions can process concurrently

The I-Unit controls the registers:

Registers	
User GPRs Control Regs	IBM POO
System GPRs System Regs	ALTA POO

Dual copies of the system and user GPRs are maintained in LSI on EA and PC MCCs.

Process Control - handles extraordinary events such as interrupts. When necessary, PC logic takes over the pipeline and initiates instructions to perform a task. Functions include PSW swaps.

Timer Facility - four timing functions:

TOD
Clock Comparator
CPU Timer
Interval Timer
} All updated every 125 nanoseconds.

An additional System Timer is used only by Macrocode.

E-Unit

The E-Unit has three components:

Unit		MCC	Slot Upper	Slot Lower
Decimal Unit	DU	PC	4	14
Floating Point	FP	FP	3	15
Fixed Point	FX	FX	6	12

Only one component is active at a time.

Decimal Unit - handles decimal operations like add, subtract, multiply, divide, compare, and shift. DU also performs Move With Offset (MVO). All instructions executed by the DU have operands which come from storage (as opposed to registers) and results which are written to storage.

Floating Point - with one exception, the FP unit handles all floating point operations. The exception is the Divide Extended (DXR) instruction which is simulated in Macrocode FAM.

Fixed Point - handles arithmetic, shifts, logical operations, moves, branches, conversions, and any instructions which require a GPR, SR, CR, or PSW to be written to. The FX unit can get operands from the I-unit registers or CPU cache.

A Bypass Path permits FX output to be returned as input for the next operation while the results are also being written to their final destination.

E-Unit Flow and Control - Each unit has an Operand Word Register (OWR) for input and a Result Register (RR) for output. If an operand is not in an OWR when required, the I-Unit pipeline interlocks until the fetch from main storage is complete.

All E-Unit components are microcoded.

CPU Storage

A Separate CPU Storage component exists for each 5890 processor. The system consists of ten MCCs:

MCC	Slot Upper	Slot Lower	Function
BUFØ	9	9	Buffer 0
BUF1	8	10	Buffer 1
BUF2	5	13	Buffer 2
CC	10	8	Cache Controller
BEL	11	7	Basic Error Logic

Functional Units:
High Speed Buffer - storage
Cache Controller - logic (CC + EA MCCs)
Error Correction - BEL MCC

Cache Functions:

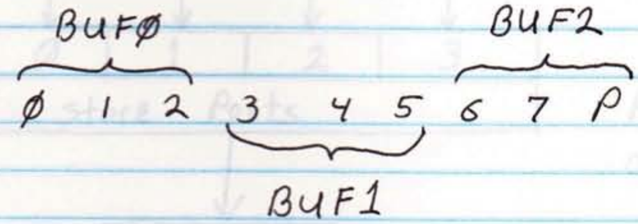
1. Provide instructions and operands
2. Store modified data
3. Match requested addresses with data in cache
4. Request data from Main Storage (via system controller).

Storage is divided into separate Instruction and Operand caches. Each cache contains <u>entries</u> consisting of 64 bytes (a line) of data plus a <u>tag</u> (system address, key, status bits).

The I-fetch holds 32K organized into 256 <u>sets</u> of entries. Both entries in a set may be examined simultaneously for greater efficiency.

The Op cache holds 64K organized into 512 <u>sets</u> of entries.

<u>Buffer MCCs</u>: Each byte of cache is distributed over all three buffer MCCs!



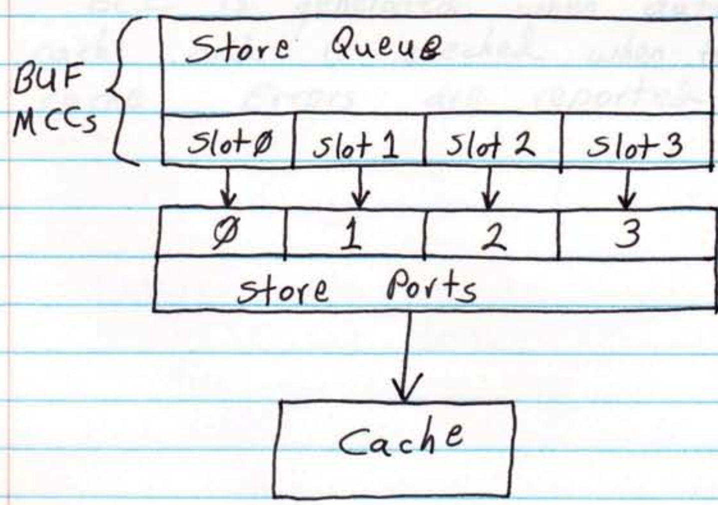
The I-Unit presents requests in the form of a real address, virtual address, or system address. Addresses in the cache are system addresses. Therefore, address conversion is usually required.

Translation occurs through DAT, a microcoded operation of CC, where the virtual address is converted to a real address and then the prefix and domain values (PFX/DBA) are used to calculate a system address. This process can cost up to 17 machine cycles.

A TLB of translated addresses is maintained to avoid repetative translations. The TLB holds 256 entries (virtual- system pairs).

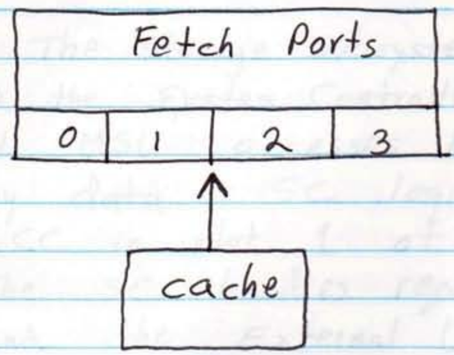
If a requested line is in cache, a cache hit occurs. Otherwise, a line missing condition causes a request to be presented to the system controller.

The cache controller is a microcoded processor with the flexibility to handle interrupts in a priority order.



Slots hold data to be written into cache.

Ports hold addresses of corresponding data.



Fetch ports hold requests for data that cannot be immediately satisfied by the cache controller. Hardware components do not have to repeat requests.

The cache controller favors I-unit operand requests. Requests to read cache have priority over requests to write into cache. Instruction pre-fetching is a low priority activity.

CPUØ cache handles data moving between storage and the External Unit (thence to IOPs) as well as data for CPU Ø I-unit.

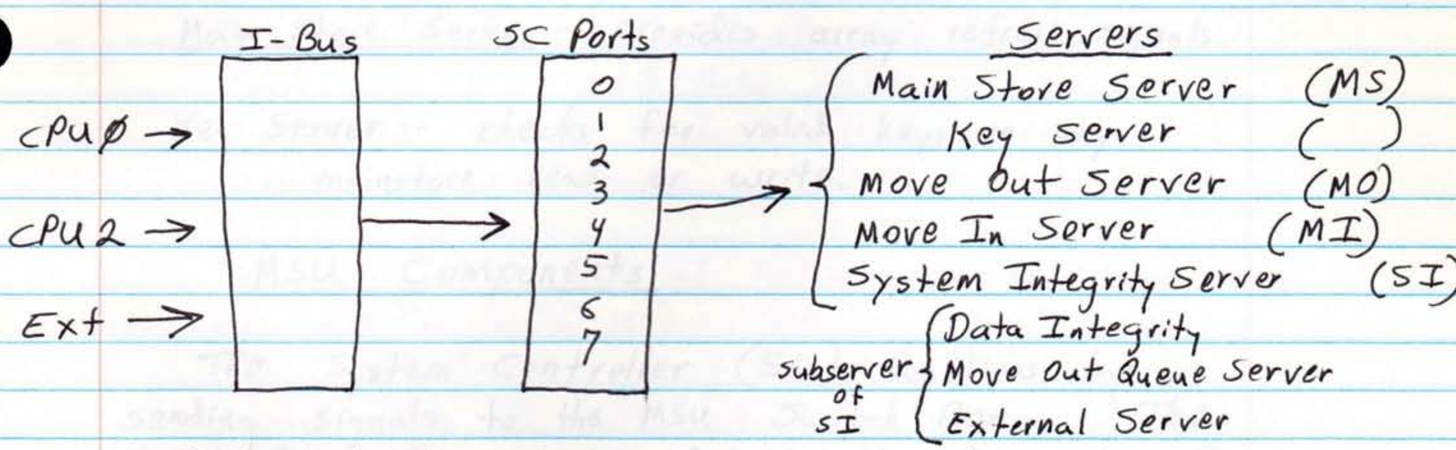
ECC is generated when data moves into the cache and is checked when the data leave cache. Errors are reported to the BEL MCC.

- Storage Subsystem -

The storage subsystem consists of the MSU and the system Controller (SC). The SC controls all MSU accesses but does not itself pass any data. SC logic is resident on the SC MCC in slot 1 of the lower (UP) stack. The SC handles requests from CPU Ø, CPU 2, and the External Unit.

System Controller - consists of three parts:

- I-Bus - keeps track of MSU requests
- Ports - 8 ports for queueing requests (address, etc., not data)
- servers - 5 servers, each responsible for a different portion of a move operation.



I-Bus - tracks all MSU requests currently in progress (called BOM busy), and sets priority of requests.

SC Ports - Each of the eight ports hold a request for storage service in the form of an address plus the function desired and other information.

Servers - the servers actually process the requests in the ports. Each server works independently, performs its specified function, and sets status information in a port message area for the other servers to use.

Data may exist in the MOQ (Move Out Queue - component of MSU), Cache Ø, Cache 2, MSU array, or be in use by the External Unit. The SC is responsible for meeting a request with the most up-to-date copy of data. Public data is read only and may be used by several hardware components concurrently. Private data, however, can be modified so only one copy may exist. Data Integrity functions are the responsibility of the System Integrity server.

Move Out server - There are two types of move outs:

Long Move Out - data is moved out of the cache and placed in the MOQ

Short Move Out - cache located is invalidated without moving the data.

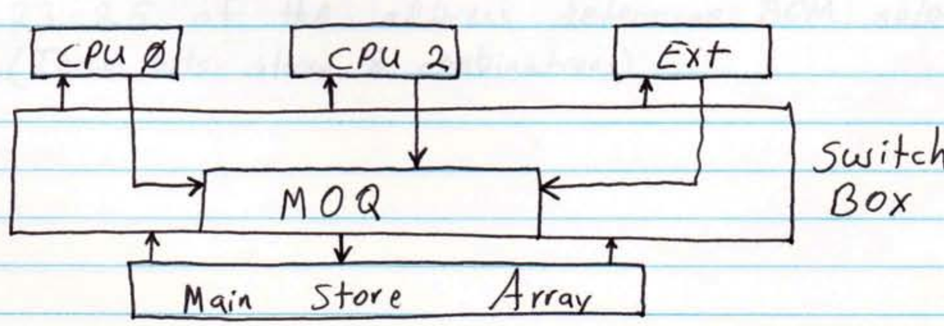
Main Store Server - provides array refresh signals.

Key Server - checks for valid keys on any mainstore read or write.

MSU Components

The System Controller (SC) functions by sending signals to the MSU Switch Box. The Switch Box also provides data paths from the CPUs, External Unit, and MOQ.

The MOQ is a special component of the switch box which holds data to be written into the array cards. The MOQ permits data reads to take priority over data writes.



The MSU has three functional components:
- Switch Box
- Key Facility
- Main Store Facility

Key Facility - contains logic and storage for protection keys. It is composed of one Key Control BCC and one Key Array card which holds the keys. Key Control functions in response to the Key Server in the SC.

Main Store Facility - provides storage and addressing logic.

Physical Components - All MSU components are implemented on the swing gate with either LSI or non-LSI technology.
The Switch Box consists of one Switch Control card and 8 Switch Data cards (SWD). The SWD cards transfer data in 16 byte paths and contain the MOQ array.

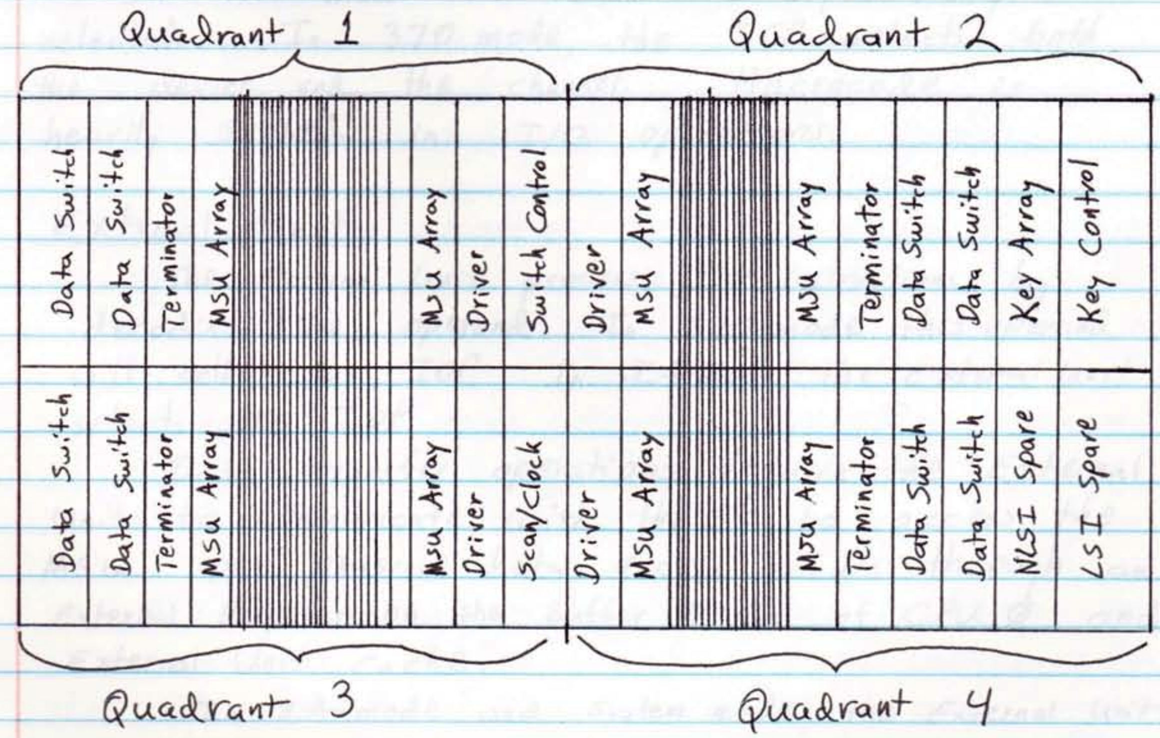
Main Store consists of 80 array cards (total capacity is 256 MB) which are divided into four quadrants. Each quadrant contains 20 array cards, 2 SWD cards, one address driver card, and a terminator.

Main Store as a whole is organized into eight (Ø-7) Basic Operating Modules (BOMs). Data are Organized into 64 byte lines. Consequtive line addresses will reside on consequtive BOMs. Bits 23-25 of the address determine BOM selection. (Three bits allow 8 combinations).

Each BOM may write either 64 bytes (a full line) or 32 bytes (a half line, sent by the I/O subsystem).

The actual data for any line of storage is spread over all 80 array cards.

Memory Errors - ECC is generated for each 16 bytes of data. Also, an M-bit sets parity between the MOQ and the MSU array. Single bit errors are corrected in the MSU. Multi-bit errors may be isolated to five BLCs. The MSU Theory of Operations Manual describes multi-bit isolation.



I/O Subsystem

Components :
- External Unit (supports up to 4 IOPs)
- IOPs (Supports 16 IHs)
- Interface Handlers (2/BLC; Dual Density IHs)

I/O Processing :

CPU - Decodes an I/O Instruction
External Unit - Selects the channel path and initrates processing by the appropriate IOP. Requests data from SC.
IOP - Controls data transfer
Buffers data
IH - Controls device selection and data transfer
Buffers data

The interrupt is passed through the IOP to the External unit which presents it to a CPU.

In XA-mode the channel is dynamically selected. In 370-mode, the SCP selects both the device and the channel. Macrocode is heavily involved in I/O operations.

External Unit

The External Unit processes I/O instructions by decoding the operand. In 370-mode this operand will select the IOP. In XA-mode, the External Unit selects the IOP.

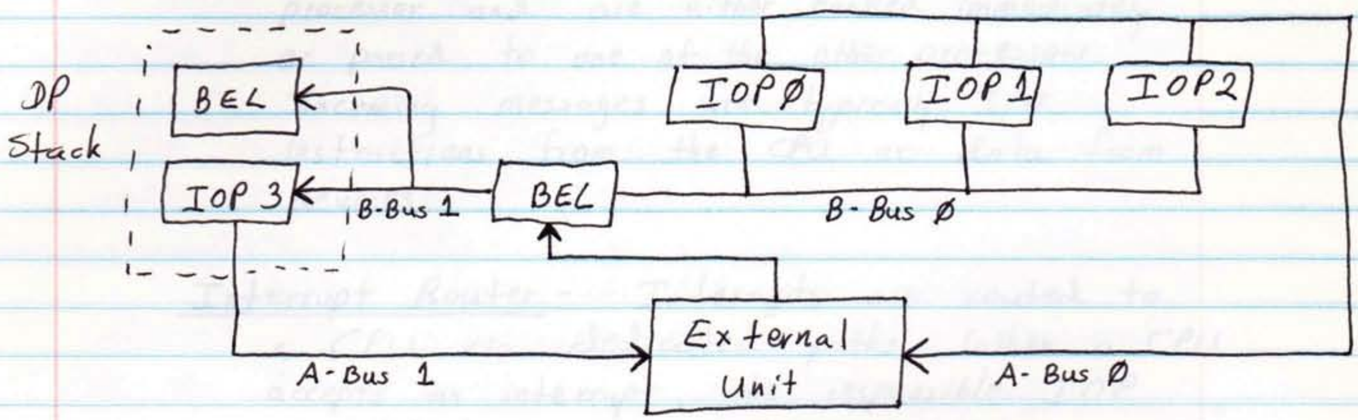
Data transfer operations require the External Unit to communicate with the SC to access the MSU. This physical data access occurs through an External Register on the Buffer MCCs of CPU Ø and External Unit cache.

In XA-mode and system mode, the External Unit maintains a queue of pending I/O interrupts. For 370-mode I/O, this queue is kept in each IOP.

Because the External Unit makes path selection in XA mode, it keeps the status of all I/O devices (via HSA).

Finally, the External Unit provides clock synchronoization between the I/O subsystem and the rest of the 5890. This occurs because the CPU clock speeds are faster by a ratio of 2:3.

Physical Locations - the External Unit is resident on the EXT MCC in slot 2 of the lower stack. The EXT communicates with the IOPs via two uni-directional buses.



The BEL MCCs supply power for the B-Bus.

Operation - the External Unit is a small processing system. It has three task processors: Work Processor, Interrupt Router, and Message Screener. A Processor Complex Register File (PCRF), a Message File, and Cache provide storage. The Channel Configuration File (CCF) stores a configuration map in RAM.

The External Unit receives messages from its IOPs on the A-Bus, and issues messages to the IOPs on the B-Bus. Both data and control signals travel on the buses. Each bus is 8 bytes wide.

These buses do not extend to the CPUs or System Controller (SC). External Unit messages from the CPU are delivered over an M-Bus. Messages from the External Unit to a CPU follow the same path as data flowing from the External Unit to the MSU. However, control signals inform the CPU that the data is really a message, an I/O interrupt, for example.

Ext Processors:

Message Screener - messages off the A-Bus and M-Bus are examined first by this processor and are either handled immediately or passed to one of the other processors. Incoming messages are typically I/O instructions from the CPU or data from devices.

Interrupt Router - Interrupts are routed to a CPU via dedicated paths. When a CPU accepts an interrupt, the responsible IOP is notified via a B-Bus message. XA and System mode interrupts are queued by the Interrupt Router.

Work Processor - this is a microcoded processor which functions chiefly in support of XA I/O operations. It tracks the work to be done, performs XA path selection, maintains channel path status in the HSA, and performs SIOF subchannel queueing for 370-mode I/O.

IOP Operation - Each IOP resides on an MCC:

MCC	Stack	Slot
IOP Ø	Lower	4
IOP 1	Lower	5
IOP 2	Lower	6
IOP 3	Upper	12

Each IOP can support a maximum of four byte channels.

An IOP consists of: I/O Controller (IOC) and Bus Handler (BH).

IOC - is a micro and nano-coded barrel processor with 16 slots. The IOC controls both the Bus Handler and the IHs. During each IOP cycle and new channel gets a micro instruction started. Each instruction completes in eight cycles.

A barrel slot represents one system channel (not subchannel. Conversion was performed by the External Unit).

Bus Handler (BH) - serves as the interface between the IOC and the A-Bus, B-Bus, and IHs. Data and signals are held in BH RAM. Each IOC slot owns a unique work area in BH RAM. Also, the Command Status File (CSF), and Data Status File (DSF) reside in BH RAM.

Data Flow - during a read, data is placed in BH RAM by the IH (DDIH). A message to the External Unit is then sent which causes the data to be retrieved from BH RAM, buffered in the External Unit, and then forwarded to the MOQ under the control of the SC.

The data transfer, once underway, between the device and BH RAM occurs under the control of the DDIH without direct IOC involvement.

Dual Density Interface Handlers (DDIHs) - the IHs manipulate tag lines to control I/O devices and buffer data. Any device connected to an IH must conform to IBM I/O specifications.

Types - there are two types of DDIHs:

Block / Block - has a 256 byte buffer, split evenly between the two IHs. can function in either interlock or data streaming mode.

Byte / Block - on this type of DDIH, one of the IHs functions as a byte mux channel. The Block IH has 128 bytes of buffer; the byte IH has an 8K buffer (32 bytes for each of 256 devices). The byte IH can operate in either burst or byte interleave mode.
The byte channel must always be the odd numbered channel of the pair.

Data Flow - a DDIH is connected on one side to a device control unit. On the other end it connects to BH RAM. A Block/Block DDIH has a single data path between the BLC and the BH. A Byte/Block DDIH has two data paths between the BLC and the BH.

Data movement in and out of IH buffer storage occurs under the direction of an In Pointer for writing data, and an Out Pointer for reading data.

Hardware Storage Area (HSA) Control Blocks

The HSA resides in the uppermost two megabytes of real memory. The space occupied by control blocks in the HSA depends on the size of the I/O configuration.

One index into HSA control blocks is maintained in the HSA itself. Another resides in External Unit RAM.

HSA control blocks are built using information contained in the IOCDS.

Subchannel Control Block (SCB) - stores information about a device. This includes device status, ISC, channel status, device number, and unit address. In 370-mode, a device with multiple channel paths will have one SCB for each path. In XA-mode, only one SCB will represent the device and other SCBs are disabled.

The information in the SCB is available to the SCP. The Store Subchannel (STSCH) instruction causes Macrocode to format the SCB data into a SCHIB. The contents of the SCB (like the ISC) may be modified by the SCP via the Modify Subchannel (MSCH) instruction.

Logical Control Unit Control Block (LCUCB) - describes a control unit, listing type, paths, and devices which have pending operations. The External Unit accesses the LCUCB when making dynamic path selection decisions in XA mode.

Device Address Lookup Table - (DACT) - maps a physical IOP slot number and physical unit address to an SCB and a specific path attached to an SCB. It is used by an IOP to located an SCB. Each DACT entry is four bytes long.

I/O operations are directed to device addresses. The SCP may reference device numbers. Macrocode can display an SCB number when given a device number. Then, ACS may be used to display the contents of the SCB. The device address may be obtained from information in the SCB and LCUCB.

I/O Instruction Processing -

CPU - SSCH instruction causes FAM entry into macrocode. Macrocode locates the SCB using SSCH operands and sets start operation status. Macrocode executes a Request Subchannel (REQSCH) which is sent to the External Unit.

External Unit - Message screener receives the message on the M-Bus.
The Work Processor fetches the SCB and associated LCUCB. The LCUCB is searched for a free channel path. Then, a REQSCH message is generated for the appropriate IOP (using the channel path ID in the LCUCB and the map in EXT CCF RAM).

IOP - the Bus Handler receives the message on the B-Bus and places it in BH RAM for a given slot.
The IOC fetches the SCB and the CCW. It sets registers in the IH for length of data and device address (using the SCB).

IH - engages in device selection and data transfer until the byte count is zero. Then it generates an interrupt for the IOC.

IOC - places status information in the SCB and informs the External Unit via bus message that the IOP is free.

The IOC sends a "Post XA Interrupt" message to the Interrupt Router.

External - Interrupt Router queues the interrupt. The status pending condition is cleared after the CPU issues a TSCH or CSCH instruction.

Console Subsystem

The console subsystem consists of two processors. The Console Support Processor (CSP) is the lower-level control system. The System Support Processor (SSP) runs ACS. Both processors are physically located on the console MCC.

SSP Components:

- Processor (IOC)
- Storage (CSU)
- I/O Devices (floppy + hard drives)
- Display Terminals
- Modem
- CSP interface

SSP Locations:

The console storage unit (CSU) is implemented on BLCs in the SSF:

BCC	Slot
Peripheral Interface (PI)	2∅
XMEM	17
Drivers	9, 1∅
Memory	5, 6, 7, 8
ECC Array card	4
Terminator	3

The XMEM card holds PROMs for both the SSP and the CSP. The PI BCC boosts signal levels for remote devices. Memory is implemented on five CSU array cards: four for data and one for ECC.

CSU contains four megabytes. Each slot in the IOC barrel processor can access the CSU, (but only one slot at a time).

A CSU line of storage consists of 32 data bits and 7 ECC bits. Each line of data is spread over two array cards:

Group ∅		Group 1		ECC
000000 - 1FFFFF		200000 - 3FFFFF		
Bits ∅-15	Bits 16-31	Bits ∅-15	Bits 16-32	Bits 32-38

Driver BCCs

Bits ∅-15 32-35	Bits 16-31 32-38

The IOC is an 8-slot barrel processor. Each slot has a working storage area and exchanges information through a mailbox storage area.

Each microinstruction is processed in eight cycles.

Slots

Ø - Executes microcode which emulates a 370-mode processor. ACS and the microcode monitor are executed by this slot.
1 - Timer
2 - Hard Disk and Floppy Drives
3 - Modem
4 - Device Emulation
5 - SAM / Resets / Logouts
6 - Terminal
7 - Bus

SSP Interfaces:

1. Bus Interface - send + receive commands, reset channels, alter and display memory.

2. Scan Interface

3. Console Immediate Control (CIC) - resets, clock control, + SAM. This functions by reading 6 IDRs and 6 ODRs.

Console Support Processor (CSP)

The CSP is the lower-level processor. It initializes and loads IOC microcode and can display and alter SSP latches, registers, and storage. In addition CSP can margin the 5890 oscillator.

The CSP consists of six chips on the console MCC plus two PROMs on the XMEM BLC. It uses the PI BLC to communicate with the terminal and maintenance panel. CSP cannot access the floppy drives. CSP firmware is updated by replacing PROMs on the XMEM BLC.

CSP is controlled via a limited set of commands which consists of PF keys, single-letter commands, and ALT/letter commands.

During console IMPL, CSP begins execution with PROM location ØØ. It executes a hardware self-test, loads SSP microcode, and then loads the microcode monitor. The microcode monitor loads ACS which, in turn, loads microcode for other 5890 components and loads macrocode.

CSP status during IMPL may be displayed on line 25. With the FE key off, only an error condition will cause a display. With the FE key on, status is continually displayed. The right-most digit of the status indicates storage errors:

B - PROM address parity error
D - PROM double-bit error
E - PROM single-bit error

Should IMPL fail, line 25 may contain the only diagnostic information.

CSP screens may be used to display and alter SSP latches and memory. Consult the <u>5890 Control System Field Reference Manual</u> for details on CSP displays. SSP latches may be stored in CSP RAM for later examination.

Minidisk backups are done by IPLing DMS from the microcode monitor. Place the DMS floppy in a drive and select this as the IPL device via ALT/T.

Microcode Monitor - during a normal IMPL (FE key off), the microcode monitor automatically brings up ACS. It may also be used to alter and display SSP registers, PSW, and storage.

The microcode monitor code is loaded into IOC control store by CSP from a PROM on the XMEMBLC.

Screens:

Line 1 - Status. The contents of this line may not be directly modified. This line includes an IPL field indicating the source of ACS:

- D = hard disk
- Ø = Floppy drive Ø
- 1 = Floppy drive 1

Line 2 - PSW - may be modified

Lines 3 + 4 - GPRs - may be modified

Lines 6-21 - CSU memory. Memory addresses are displayed on the left. To display a particular location, type the new address on an address line. Any memory location may be modified.

Commands:

- ALT/C - Clear console memory
- ALT/D - Toggle debug mode
- ALT/I - IPL ACS or Diagnostics
- ALT/R - Restart PSW
- ALT/T - Toggle IPL device
- ALT/up arrow - Start console CPU
- ALT/down arrow - Stop console CPU
- ALT/EOF - Idle the monitor

Once ACS or the microcode monitor are active, CSP screens may be displayed on the terminal by pressing the IMPL button (with FE key on).

To swith between the microcode monitor and ACS, use the ACT/EOF key.

ACS

ACS code resides on the hard disk, is loaded into CSU, and executes on the SSP. ACS can run applications such as Log Analysis, Scan Machine, and diagnostics as well as built-in commands.

Functions:

- 5890 Resets
- Load microcode
- Load macrocode
- Maintain configuration
- Track 5890 resource utilization
- Supports modem hook-up
- Diagnoses 5890
- Performs error recovery and logging
- Performs device emulation.

ACS Files: the hard disk is organized into a fixed number of logical units called mini-disks. A root directory points to each minidisk. Each minidisk, in turn, has a directory of its contents. It may also contain sub-directories.

Each floppy drive is treated as a minidisk. The ATTach Ø|1 and DETach Ø|1 commands control physical access.

Minidisks

Directory Name	Contents
Ø	Root directory
DriveØ	Floppy drive Ø
Drive1	Floppy drive 1
Alt	Alternate copy of ACS
Page	Scan page formats
uc	microcode
log	machine, channel check logs, ACS event log
mlevel	
user	Customer working area
CPROCS	CPROC files
Conf	Hardware configuration files
Docs	Help files
Diag	
Sys	Macrocode files
XAData	IOCDS files
Dump	Main storage dumps

When the FE key is off, the current directory is /User. When the FE key is on, the default directory is /CPROCS.

To access a file under the current directory, simply use the file name along with a command. If the file is in another directory or sub-directory, specify the path along with the file name.

For a file within a sub-directory:

directory-name/file-name

For a file in another directory:

/directory-name/file-name

For a file in another sub-directory and directory:

|directory-name|sub-directory|file-name

The IDiag minidisk uses many sub-directories.

Each file has protection attributes. As a rule, never attempt to alter a file unless its directory is the current working directory.

File Commands:

Q DISK [FREE] - lists each minidisk, directory name, physical disk location, size, free space, and attached status (R/W). The NAME of a minidisk may not be identical with the DIRECTORY name on the disk.

LST [L S] [directory-name] - list the contents of the current directory or the directory specified.

PWD - Print Working Directory: simply displays the name of the current directory.

CP - copy file

CPT - copy all files in a directory to another directory.

MV - move file (functions as a rename).

CMP - compare files

CD - change current working directory.

ACS Keyboard Operation

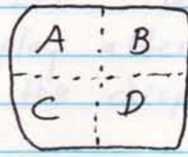
PA1 - clears the command line

PA2 - Cancels the current process

ALT/ATT - redisplays the last command

ALT/PA1 - restarts the ACS keyboard handler to clear a locked keyboard.

The ACS screen is formatted into quadrants:



ACS commands are assigned to one of three privilege levels.

C - general
B - requires FE key on
A - requires FE key on and may only be issued from the master console (REQ command).

Multiple ACS commands may linked together with slashes (/) and entered on a single line. Command options may be displayed using ? after the command. HELP is also available.

Command categories:

- File system
- Alter / Display
- Query / set
- Enable / Disable
- CONFiguration
- Install
- Scan
- System Modification - loads, resets..
- SAM
- AMDAC
- CDM - console diagnostic monitor

The contents of a display may be saved by selecting a "user screen" and then displaying something. The screen image is then saved to disk.

Other commands:

ENABLE AUTOVERIFY - updates a configuration or memory display after a change without having to re-enter the display command.

EN RDP STATUS - permits continuous update of the status line. Updates occur once per second.

CLR - clear screen

RETRIEVE - redisplays the last command.

ACS Scan

The scan facility involves reading and setting 5890 latches for diagnostic purposes and setting all 5890 latches to a predetermined state during a reset.

Scan page formats are stored on the lpage minidisk. These are documented in the Scan Page Reference Manual.

The ACS command:

D PA page-number Q_x

causes a specified scan page to be displayed into the designated quadrant. The display command selects the scan page of the current CPU. To view a scan page from the other processor, use the CC command prior to the display.

D PA 22 QA/CC 2/D PA 22 QB

Scan pages are grouped into 64 scan pages. Four Pages are assigned to each screen and may be displayed with the command:

D S#

↑ screen number

The assignment of scan pages may be viewed with the command:

Q SSA

and may be temporarily superseded simply be displaying a scan page on top of an already displayed scan screen. This assignment will last until the next ACS IPL. To restore the original settings, enter the command:

RST SSA

To permanently change the Scan Screen Assignment, use the command:

SAVE SSA

Logs - Machine Check Logs consist of all 5890 latches stored in scan page format. The command:

ENABLE LOG #

causes all subsequent scan commands to be directed at the stored log. When done, issue

DISABLE LOG

to stop looking at the stored latches. Scan commands then act on the real 5890 latches.

Scanin Facility - permits any 5890 latch to be changed. Also, pressing PF12 while Scanin is function will list the physical location of any latch.

A related facility, Fast, permits scan screens to be accessed quickly via PF keys.

Scan DB - the scan database minidisk contains all of the latch settings for each component of the 5890 to be used for a reset. This minidisk will be updated synchronously with the hardware.

Display / Alter

D MSG - displays pending ACS messages. A + or - may be entered to scroll ten lines at a time.

Displaying Registers - 5890 must be stopped

D CR - displays control registers.

D F - displays Floating Point Registers.

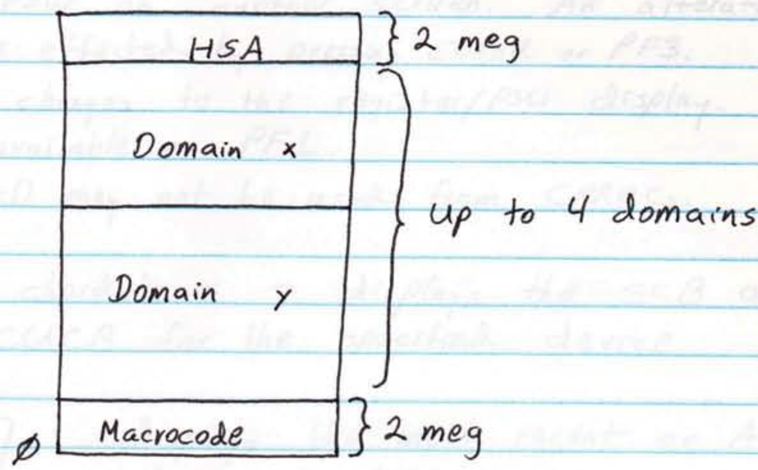
D SR - displays System Registers

D GPR - if clocks on, then displays the system GPRs.
- if clocks off, then displays the system Registers! - like D SR

D UGPR - displays user GPRs, which may be either in use by a domain or macrocode. To see domain registers, view through Macrocode. This command is mostly used when running diagnostics.

D PSW - displays the PSW on line 22. The 5890 must be stopped.

Displaying Memory



D M addr - displays absolute memory.

D M DMx addr - displays real address within the specified domain.

D V DMx addr - displays the virtual address within the specified domain.

D PSM - displays storage around the address in the current PSW.

Of the many operands which may be specified following the memory location address, two are note worthy:

I - formats the memory into assembler mnemonics.

NOText - eliminates the EBCDIC translation and increases the amount of storage displayed on a screen.

AD Process - AD is an ACS utility process that facilitates Alterations and Displays. PF keys function as commands. AD displays two sections of memory on a single screen, plus registers and PSW on another screen. An alteration may be effected by pressing ENTER or PF3. PF11 changes to the register/PSW display. HELP is available on PF1.

AD may not be used from CPROCs.

D DACT chpid-dev# - displays the SCB and LCUCB for the specified device.

D MSE [A] - displays the most recent or Accumulated main store correctable errors.

D HSB - indicates the presence of parity errors in the HSB.

Query Commands - usually provide information about ACS as opposed to the display commands which usually report on hardware.

SET PFx "string" - assigns a value to a PF key. The double quotes are required.

SET PFx "#string" - assigns a delayed command to a PF key. The # is literal and resides within the quotes.

Q PF - displays settings for PF keys 1 - 12.

Q PF High - displays settings for keys 13 - 24.

Logs - ACS stores a maximum of ten (Ø-9) machine check logs, and 100 (Ø-99) Channel Check logs. Each is time-stamped.

Q LOG [ALL] - displays ALL ten logs and marks the most recent with an asterisk.

Q CLOG - displays the most recent CLOG.

Q CLOG ALL - executes a utility that permits scrolling through the CLOGs.

Q STAT - provides an expanded version of the line 25 status information.

Q STAT PCM - displays a record of power and cooling irregularities.

Q OSL VERIFY - displays and verifies the operating state latches.

Resets - exist in an hierarchy. The most comprehensive is:

RS PO - reset power on performs about 30 steps which initializes all latches and loads microcode and macrocode.

RS COnf - reset configuration. This command does not reload microcode or clear the TOD clock. This command may be used to rebuild the HSA after introducing a hardware configuration change.

The P operand causes each reset step to be printed to the screen as it is performed. The L operand will list the steps without performing them.

RS SYS - reset system: performs a reset without altering memory or GPRs. This command may be used before restarting Macrocode.

RS SYS C - clears memory as well, thus bringing a new copy of Macrocode and rebuilding the HSA. This command is equivalent to RS CO.

RS IO [chpid] - resets all chpids or a specific chpid.

Loads

IMPL - loads microcode (explicitely).

LMP - permits loading microcode to an individual component.

IML [C] - reloads Macrocode and optionally clears memory as well.

IPL - may be used to load a stand-alone diagnostic. This is seldom used.

LDMEM - used to load a diagnostic into 5890 mainstore. Example:

LDMEM -d Ø luser/dirt

loads the diagnostic Dirt on the luser minidisk into domain Ø storage.

Clocks - The 5890 has gated clocks, free clocks, and I-unit clocks. The free clock refreshes memory and is not usually turned off. The gated clocks may be turned off with the command:

CL OFF

Once off, the clock may be stepped with the command:

CL

The SET CYCLE COUNTER (S CC) command provides even greater flexibility in controlling system clocks during diagnoses. Use of this function is described in the 5890 Control System Field Reference Manual.

Logs - a machine check log may be manually keyed with the command:

LOGK

This command might be used during a checkstop error.

ACS Maintenance

ACS maintains a configuration for memory, IOPs, CPUs, and channels. To do this, three screens are available which greatly simplify the configuration process. The commands entered while displaying the three screens are automatically saved in a disk file. This file is accessed during resets and the contents are later loaded into memory for dynamic access.

The three configuration frames, SYS, IO, and REG, list the current settings at the top of the screen together with the configuration commands at the lower portion of the display.

Configuring I/O

The command IO displays the frame. The frame lists each (of four) IOPs with each chpid. The status and type of each CHPID is displayed.

Commands - listed in order of use:

CONF IOPx ON - indicates that the specified IOP is available to the system.

CONF CHPID x - Each CHPID must be identified as byte or block and whether 370 or XA mode. A byte channel may only be configured to an odd slot of an IOP, and that slot must have a byte DDIH installed. Violation of these rules will cause an * to appear in the TYPE field for that CHPID.

CONF IOCDS xxx - ACS identifies one of the four IOCDS files to be called |XADATA| HSA. This file is used to build the HSA control blocks and must be present to reset the 5890.

CONF XA OFF - On the ACS level, this must be set OFF. Later, Macrocode will determine the correct setting to use when running a domain.

CONF OSI - determines the beginning device address (two digits) of the four possible OSI devices.

RESET COnf - this reset command writes the changes to the disk file and performs the machine reset necessary to implement the configuration.

Configuring SYS - this frame assists in defining memory, CCA, and Processors. It may be displayed via the command SYS or Q CONF SYS.

CONF MSU xxx - defines the total amount of memory in megabytes.
CONF HSAB xxx - this command defines the HSA base address (lower). To provide for two megabytes, subtract X'200000' from the maximum address and round up by 1. For example:

FFFFFF - 200000 = FDFFFF
FDFFFF + 1 = FE0000

CONF CCA - defines a channel-to-channel adaptor.
CONF CPU# - configures a CPU online or offline.
RS COnf - the reset command must be used to implement any configuration changes.

Configuring Registers - these data need not be modified when installing a system.

OSI Devices - the CONF OSI command defined the beginning device address (two digits) of the four devices. To actually use these, the IHCU must be physically cabled to a byte channel. Also, the SCP must define the addresses as 3277 terminals. Similarly, the ACS SET OSI command must be used to identify each address with a device type (3277) and a display station:

```
CONF OSI 90
SET  OSI 90 3277 DS1
SET  OSI 91 3277 DS2
  :
```

Install Commands

The part numbers and revision levels of microcode and all FRUs is manually maintained on files on the lmlevel minidisk.

In addition, another file on the lconf minidisk records part number and revision level for:

- FRUs
- Microcode
- Scan Pages
- Scan Data Base
- ACS
- Macrocode
- Patches
- Diagnostics

This parts number file on lconf is used by a Corporate application called the Compatibility Checker. The program compares the contents of the Parts Number File with the Machine Level Compatibility (MLC) data base. The result is a listing of any components that must be changed to avoid a conflict with some other change.

The Parts Number File may be transmitted to Corporate via floppy disk, Amdac link, or alternatively, the copy at Corporate may be edited directly. This latter method is most convenient for small changes.

Fortunately, the Parts Number File on lconf may be automatically updated.

The file on lmlevel may be updated with two ACS commands: INSTALL FRU and INSTALL UC. Upon entering these commands, ACS presents a full-screen display of part numbers. The cursor may simply be moved to the appropriate entry and new data typed in over the old. An * must be used to indicate that a particular part is installed.

ACS accesses this file when performing resets, and loading microcode. Also, the assignment of byte and block channels must match the appropriate DDIH types listed.

The Parts Number File on lconf is manipulated with a different set of ACS commands:

INSTALL VERIFY - instructs ACS to read the levels from the FRUs and compares this data with the lmlevel file. If the hardware and the file match, then the lconf file is similarly updated. If the hardware and the lmlevel file disagree, no update of lconf takes place, and a discrepency message is issued.

INSTALL INIT - this command will only be used to rebuild the lconf file in a situation where the original was destroyed and is not recoverable. In such a case, this command would generate a file and the INSTALL VERIFY command would subsequently be used to complete it.

INSTALL QUERY - will list part numbers and levels for all or a portion of the data base.

File Installation

The ACS commands used to install software also perform an automatic update of the Parts Number File in the lconf minidisk.

Do a RS PO before INSTALL CLEANUP.

INSTALL FILE - copies a new file from a floppy disk to the hard disk, renames the old version to provide a backup copy, makes a log entry of the change, and alters the Iconf Parts Number File.

INSTALL LIST - this functions similarly to the above, except that an operand points to a file containing a list of INSTALL commands. For small tasks, the INSTALL FILE command is appropriate. For more involved work, such as installation of Macrocode and diagnostics, this command is used.

INSTALL SAVE - copies all of the <u>old</u> files to a floppy drive and deletes the copies on the hard disk. This should be used to release space after a change has been proved to be reliable.

INSTALL CLEANUP - <u>deletes</u> all of the <u>old</u> files without making a backup copy.

INSTALL UNDO - reverses an update. The <u>old</u> files are returned to current status.

Check the <u>5890 Control System Field Reference Manual</u> for the exact syntax and operands available with these commands.

To determine which patches to apply to a machine, check CPS Partnumber Analysis or

EX 'JHLØØ.CMD.CLIST(QPATCH)'

Patching

Minor changes to Microcode, ACS, and Macrocode may be done by patching the existing module. A major change involves replacing the entire module and will always be done with the INSTALL command.

Patches are available on floppy disk or in hardcopy from HWS or a TIB.

Patching from Floppy Disk:

ATTach x - attach the floppy drive

LST L/Drivex - list the contents of the directory on the patch floppy to find the list file.

INSTALL LIST ALL - assuming ALL is the name of the list file, ACS will execute the commands found therein. These will include copy statements to move the patch files to the appropriate minidisk plus the PATCH commands to actually apply the updates.

When these tasks are complete, simply test the update and backup the altered minidisks.

Manually Patching: If a patch arrives via HWS or a TIB, then it must first be placed in a file on the hard disk. This is done using the ACS EDitor. ACS and microcode patches are placed in the /CPROCs directory; macrocode patches reside in the /sys minidisk.

The file created on disk becomes the operand to the PATCH command. The patch file itself contains all of the information necessary to identify the target file.

PATCH filename

Patch processing verifies that the change may be made, applies the change, and updates the /conf Parts Number File.

PATCH patchfile VERIFY - determines whether a patch may be applied without actually making a change.

PATCH UNDO patchfile - reverses a patch.

PATCH systemfile H - produces a detailed patch history of the specified file. Output is to the screen and /cprocs/patch_audit.

PATCH systemfile S - produces a summarized patch history.

Patch Contents:

The text of the patch includes a part number, coreq and prereq patches, a type (microcode, macrocode, ACS) field, the complete path name of the file to be modified, the old and new data, and finally a checksum.

Disk Management System (DMS) - is a utility which runs under the Microcode Monitor to install ACS and perform backup/restore operations of minidisks. DMS resides on a floppy disk. When invoked, it presents a menu of options:

Restore
Dump
Initialize
Configure
Track Ø
End

Minidisks which will be the object of a DMS RESTORE must first be configured. Thus, to install ACS for the first time, the first step after invoking DMS would be to configure the primary minidisk. The size of each minidisk area is predefined to DMS and would not normally be changed.

Once ACS is restored to the primary minidisk it may be used to restore other minidisks. However, prior to invoking ACS restores, these other minidisks must first be initialized by DMS.

The DMS dump option allows the creation of backup floppies of any minidisk. Make a backup any time the contents of a minidisk is changed. Label the backups properly and clearly; and keep them where they may be readily accessed in case of an emergency.

Installation Steps:

- DMS Initialize and configure
- DMS Restore of ACS, microcode, scan pages, database files, and diagnostics
- IMPL - bring up ACS & load microcode
- ACS Install of remaining files - update part numbers
- ACS Patch
- ACS CONFigure
- ACS copy of IOCDS
- IML Macrocode
- Update IOCDS
- Create & Save Domains
- Modify Autoact function list
- Activate Domains
- IPL customer

Macrocode

Purpose:

1. Provide error recovery for machine or channel checks.
2. Provide IBM compatibility
3. Provide unique features (like MDF).

Macrocode is software that is loaded by ACS into the lowest two megabytes of main store and executes on the 5890 processor.

Compatibility of instructions is provided by I-unit microcode and by macrocode instruction simulation.

Operating States:

Control State
- System Mode
- Fast Assist Mode (FAM)

User State
- Problem
- Supervisor

When the 5890 is running in User State the programs may executed the IBM defined instructions, and have access only to the IBM registers.

In control state, macrocode has access to two additional sets of registers: System GPRs (macrocode work registers) and the System Registers (containing domain characteristics). Macrocode can execute ALTA instructions as well as IBM instructions.

Macrocode in control state has two operational modes: System and Fast Assist. FAM is entered for instruction simulation directly from I-unit microcode. System State is used to handle machine and channel checks as well as other macrocode house keeping functions like interrupt handling and console communications.

The 5890 is in system mode if the I-unit flags do not indicate either FAM or user state.

Macrocode transfers control to user state from either FAM or system mode by executing either the Alta instruction RUS (Return to User state) or LPSWR (Load PSW and Return).

Domain attributes:

- Architecture: 370 or XA
- Number of Processors (LP)
- Percentage of CPU time
- Quantity of memory
- I/O resources

As domains are activated, memory is assigned from high to low.

Channels: IOCP is used to define channels, control units, and devices, and to make their relationship known to the External Unit for Dynamic Path Selection and Dynamic Path Reconnect. In 370 mode, the IOCDS supplies information required for Subchannel Queuing and Shared Subchannels.

A maximum of four IOCDS files may exist on the lxadata minidisk. These are IOCDSØ-3. The file which is actually used to build the HSA control blocks is lxadata lhsa. This file is a machine readable version of one of the IOCDS files.

The IOCDS which will be used to create the lhsa file may be designated with the ACS command

CONF IOCDS #

or with a macrocode operation.

Don't forget to DDR backup the lxadata minidisk whenever the customer creates a new IOCDS.

Channel Status - Macrocode will display the status of each system channel:

1. Installed / Not Installed - the channel is not installed via an ACS CONF command.

2. Offline - the channel is installed.

3. Not Configured - the channel has not appeared in an IOCDs.

4. Attached ("Dedicated")

5. Online

6. Unavailable - the channel has been the object of a Macrocode fence command. This prevents a domain from attaching the channel even during a reset.

7. Unusable or Not Operation - Macrocode has detected errors.

Macrocode Console -

Sys Req (ACT/ATT) redisplays the last macrocode command entered.

PA1 - clears input & returns cursor to the command line.

PA2 - clear asynchronous messages.

Macrocode Frame are grouped into functional families.

SF - System Configuration Group
- CC - Configuration Control
- CA - Configuration Attributes
- CI - Configuration I/O
- CD - Configuration I/O Display
- SR - System Resources - permits taking storage or a CPU offline. The resource may not be restored without a system reset.
- SD - System Devices - defines domain consoles, including the macrocode master console.
- SI - System I/O - lists the allocation and status of each channel. Options permit a channel to be Fenced or unfenced.

SA - System Control Group
- FC - Function List Control
- MI - System TOD
- CL - Console Log
- SL - System Log
- PF - key assignments
- SS - System Scheduling
- DS - Domain Status - reports status for each logical processor: Stop, Run, or Manual. Also indicates any physical CPU affinity.

SP - System Support
- AE - Amdahl EREP Interface
- AD - Alter/Display
- RO - Recovery Options
- TR - Amdahl Trace Control
- HC - Hook Control

DA - Domain Control
FC - Function List
CL -
SC -
PF -
DS -
OP -
OE - Operator Extended functions.

DP - Domain Support
AD - Alter/Display
RC - Recovery Options Control
DE - Domain Debugging

Macrocode Maintenance

Installation of macrocode involves moving files such as MACROA, MACROB, etc. from a floppy to the hard disk using the ACS command:
INSTALL LIST ALL
and then applying any necessary patches. The files include a macrocode load map.

Macrocode patches, like the macrocode modules themselves, reside on the /sys minidisk.
Naming:
/h#xxxxyy
where: xxxx = HWS number
yy = version number

Patches are applied using the regular ACS patch procedure.
Command format:
PATCH /sys/patchfile [H - history, U - undo, S - Summary, V - verify]

For the H and S options, the filename should be the module name rather than the patchfile.

A <u>cold start</u> of macrocode involves loading into memory a new copy of macrocode and rebuilding all control blocks. After a cold start, domains must be activated. Cold Starts occur with:

- Power On
- RS PO command
- IMLC
- RS SYS C/IML

A <u>warm start</u> involves simply re-loading a new copy of macrocode while preserving the macrocode control blocks and domain storage. Warm starts may be used to recover from errors. Warm starts may be initiated with the commands:

- IML
- IML NR - "no reset" explicitely stated

Also, an RPSW from ACS will cause macrocode to execute a restart PSW. This causes macrocode to restart without reloading any memory areas.

<u>Macrocode Diagnostics</u>

The ACS command MACDUMP transfer macrocode from memory to disk or tape. The command has options which permit domain storage to be dumped as well as macrocode.

The macrocode (TR) Trace frame activates a trace of macrocode events. Exactly which events are traced is governed by entries on the HC frame.

Macrocode may also enter a disabled wait. To determine, enter the ACS command

D PSW

and examine the wait and interrupt mask bits.

Verify that the machine is in system state by checking Scan Screen 1. If so, reference the wait state code in the PSW.

Macrocode recovery is controlled by the Recovery Options (RO) frame. For each type of error, macrocode may be instructed to stop immediately or continue. One option can even expressely prevent a warm start should macrocode attempt one.

Two logs exist covering macrocode:

1. The RO frame, option D, determines the contents of /sys/Log.Event. This file may be viewed with the ACS command:

   D_MACLOG

2. The macrocode event log is kept in the file: /log/events and may be displayed with the ACS command:

   D Events

Macrocode Files

/sys Minidisk

- Program files - executable macrocode
- Configuration files - consist of the name assigned on the CC frame with a node consisting of the literal 'CO' and a three digit number indicating the number of times this configuration has been saved. Ex: MVSXA. COØØ3
- Function Lists - reside on /sys with the name followed by 'FL' and a three digit number. Example: REIPL. FLØØ1

Log files - macrocode log.event.

Ixadata Minidisk

IOCDS files - named: IOCDS.AØ etc.
HSA - contain HSA control blocks as prescribed by a single IOCDS.

Macrocode - ACS interface -

Since macrocode uses the console hard disk, and since the disk is owned by ACS, the Write Console Commands (WCC) provide an interface. Macrocode can open, read, write, close, erase, and seek an ACS file. The response to a WCC may be an external interruption to macrocode.

Macrocode and ACS also work together in handling errors. ACS is the first to intercept an error which it logs, and macrocode may also handle the error. If required, macrocode reflects the error to the SCP.

Diagnostics

5890 diagnostics are documented in three manuals:

- 5890 Diagnostics Manual - has infomation on all diagnostics.

- System Level Diagnostics Manual - provides detailed information on Dirt, Alpha, and 8E7.

- 5890 Maintenance Manual - contains task break-downs and physical descriptions.

There are four types of diagnostics:
Console - hardware and architecture tests
Mainframe - specific hardware exercisers
System Level Tests - hardware and architecture stress testing.
Tools - engineering tests for machine development.

Console Diagnostics - all begin with the letter 'A'.

Console Micro Diagnostics - the A4ØØØ diagnostics reside on two PROMs (Data and ECC) on the XMEM BLC and run on the CSP microprocessor. The A4ØØØ test menu is invoked by pressing PF9 while in CSP.

These programs test the console hardware at its lowest level: IOC, Mailbox, CIC, CSU, terminal, + I/O interface.

CLAM - Console Loader and Monitor: this is loaded from floppy disk. Once the monitor is up, the specific tests are also loaded from floppy. Upon failure, CLAM displays the Error Screen which holds the failing address and GPRs. To trap the error, place an adstop on the failing address and rerun the test.

CLAM tests:
- A7Øxx - instruction set
- A8ØØØ - terminal test
- A8Ø1Ø - Floppy and hard disk test
- A8Ø3Ø - Scan interface
- A8Ø4Ø - Console Immediate Control (CIC)
- A9ØØØ - System Level Test - random instruction sequences + hard and floppy disk exerciser.

Mainframe Tests - each test consists of:

Test
  Test Group
    Test Case
      Test Instance

The console-based mainframe tests reside on the Idiag minidisk and are invoked through the Console Diagnostic Monitor (CDM). If the test selected is written in 370 assembler, CDM automatically invokes the X Test Loader (XLDR) to initialize the PSW, GPRs, and CRs, and then load the test into memory. CDM communicates with XLDR through the DIAGnose instruction.

CDM runs as an ACS background task and is invoked with the ACS command:

DIAG

CDM commands exist to load specific tests, cases, breakstop, halt, cycle, + loop.

CDM tests:

- B2ØØØ - Scan and Error History Log (EHL)
- B2ØØ1 - MCC Control Reset
- B3ØØ1 - Cable Plug-in Test - good after installation. Lists the part number and location of each cable.
- C2ØØØ - Control Store Tests
- C3ØØØ - GPR and FPR Tests - Dirt is better + runs faster.
- C4ØØØ - RAM Test - all system RAM including cache
- E25ØØ - MSU ECC Test
- E3ØØØ - Apache Beat - simulates I/O loading
- E5ØØØ - CCA Microcode Test

During actual problem determination the higher level diagnostics are usually executed first. Therefore, since these higher diagnostics such as DIRT usually identify the failing component, the mainframe level test will seldom be used.

Mainframe level architectural tests -

Bridge Tests - tests 370 and Alta instructions. This may be used after a RS PO works and before running the system-level diagnostics.

F3ØØØ CDP/TSS Test - CDP tests channel architecture. TSS loads into mainstore and tests architecture and microcode.

System Level Diagnostics

Dirt - Data Integrity Random Test - exercises virtual and real addressing, key checking, and I/O data transfers. Tests cache, MSU, and SC. Dirt runs either native or under macrocode.

Alpha - simulates the stress of an SCP. Test the I and E-units. The bridge tests may be used prior to Alpha. Alpha runs either native or under macrocode.

8E7 - verifies 370 and Alta architecture running in native mode.

Tools - one engineering tool useful in the field is the Channel Diagnostic Processor (CDP). This is a microprogram that executes in the IOP. It simulates two devices per slot and can run both byte and block mux channels.

The IOP running CDP looks like an I/O farm to another IOP that is actually being tested. The DDIHs of each must be cabled to the other. This is useful for testing interfaces during an installation when no I/O devices are available.

CDP can simulate up to 16 channels concurrently. F3ØØØ, Alpha, and DIRT may all be used to direct I/O to CDP.

Strategy -

If the console works, run System Level Tests.
If the console is not completely operational, run the PROM-based tests.
If the console does not work at all, follow the Console SMAPS in the Maintenance Manual.

Most console tests will indicate a failing console MCC or a BLC in the Console Card Cage.

Installing Diagnostics: the diagnostic package consists of a Disk Management System (DMS) and a set of floppies. The DMS will be IPLed and used to transfer the tests from floppy to the /diag minidisk (except CLAM test which remain on floppy).

The /diag minidisk uses sub-directories:

Diag

xldr b e c f s x bridge monitor testlist tools Rev#

- x → xyzzz, sync_tod, first_4K
- s → apb, 8e7, dirt, alpha, cdptss
- f → F2000
- c → C2000, C3000, C4000
- e → E2500, E5000
- b → B2000, B2001, B3000, B3001
- tools → xldr_init, cdpiml, cdp

If EHT is displayed on line 25, check scan page 103 (screen 1 QD) for EHT bits. If a log is not keyed, then key one.

Troubleshooting

The Scan Facility is a function of ACS. Since ACS runs on a separate clock than the 5890, it continues to run even after a clocks off error. The ACS SCAN OUT command may be used to read a latch even if that latch is not displayed on a scan page. Latches are located through scan coordinates: MCC, chip, & bit.

A Scan In of data may be performed either by using the FS command or by using the scan coordinates.

Scan pages are grouped in blocks of 100 and describe functional units. Custom scan screens may be assembled with the ACS command:

DISPLAY PAGE

Documentation includes:

- Scan Page Reference Manual - absolutely worthless
- Fiche - slightly better than worthless.
- FERM - valuable only in relation to the worthlessness of the other documentation.

Scan Page 103 is the error Histor Tree (EHT) which is the first stop when diagnosing a machine check. This page lists each functional unit and indicates error propagation. When an error occurs, a bit is set in the leftmost column for the component. With each machine cycle, the bit to the right is set. Finally, when the right-most bit is set, the 5890 stops. Only one component should have all of its bits set. Other components may have error bits set, but these are the result of the original error propagating itself.

With the failing component identified, check the first few scan pages in the block assigned to that component for more detailed information.

Before powering down via UPC, issue
CL Off
to make sure ACS is not doing any disk I/O.
Then do
RS PO
after restoring power.

The serial # of the new part must entered into INSTALL FRU file.

Log Analysis (LA) is an ACS application that analyzes all machine check logs and calls suspected FRUs. ACS automatically invokes LA. Alternatively, it may be manually invoked with the command LA. Numerous options exist to control execution.

If multiple errors are found, LA assigns a probability of failure to each. The results of analysis are display at the terminal and written to the ACS Event Log.

Machine Checks may be either hard or soft, and recoverable or nonrecoverable.

CLOGs - when a channel error is detected, a channel-logout-pending signal is passed to the Interrupt Router. The CPU then attempts to reset the channel path. If the reset is unsuccessful, the path is taken offline and flagged as permanent.

A CLOG contains:

current domain #	channel address
CRW	IOP DDIH regs.
Tags	IOP Working Store
Bit RAM.	Error Pgm Counter (EPC)

The EPC indicates the microprogram instruction executing in the failing slot at the point of error.

For additional information on chanel errors, see the report from the SCP.

ACS Log Commands:

Q LOG - displays the most current mch chk log
Q LOG ALL - displays all mch chk logs
Q CLOG - displays the most current channel log.

<u>ACS Event Log</u> - contains records of unusual hardware events:
- machine checks
- channel checks
- macrocode recovery
- power faults
- high temperature warning
- System Error Handler (SEH) invocation
- LA activation (+ results)
- MCIC

<u>Macrocode</u> - is used to troubleshoot domains by display PSW and registers, and by tracing loops.

<u>Event Log</u> - Macrocode's Event Log records activities related to the domains:
- Resets
- IPLs
- machine checks

The macrocode event log may be viewed with the command:

D MACLOG

<u>EREP</u> - analyzes machine and channel check logs, provides a formatted output, and can even call a failing FRU.

<u>Memory Errors</u> - the ACS command:

D MSE

identifies all single-bit errors by card location (bay and card).

Uncorrectable memory errors may be isolated to a set of four cards.

Data Base Files:

TIBs - notes from PSAS + support staff.
HWS - detailed problem and fix information
EWS - software problems
HATS - incidents

SMAPs (System Maps) - flow charts in the maintenance Manual to direct FRU isolation. The intention is to direct work for the first two hours. Two types:

General - for Local support
Detailed - AMDAC

The general SMAPs for console and power problems are more detailed since AMDAC support cannot be available unless the console is functioning.

Problem Management

When a failure occurs, insure that a log has actually been written to disk.

Log Analysis (LA) is not always right. After LA has called the FRU, and the part is on order, check the TIBs and HWS.

I-Unit timeouts and mainstore uncorrectables require gathering more data than is available in the logs.

The site log should contain:

- Hardware Configuration
- Compatibility Checker lists
- Domain Configurations
- Incidents
- Patches and ECs
- Problems
- Telephone Numbers

Run all diagnostics and note any discrepencies with optimum results.

5890 PM - yearly: change filters and inspect all fans.

Failure Analysis System (FAS) - this is the AMDAC hook-up process where by files are automatically transferred to Corporate. The transferred files include the Macrocode Event Log, Part Number File, and the LA Result File.

For any solid failure, run a System Level Test (DIRT) before replacing a part. This establishes whether the same diagnostic may be used to validate the repair.

Amdac - to perform a hookup, enable the Amdac key and enter:

EN AMDAC DEPOT D

When the connection is made, enter:

XFER CNTL

to transfer control to display station 5.

3/23/88

To use the 5890 as a CCC terminal:

1. Dial 1-800-345-5890

2. Enter: En Amdac Term

This presents a system D logo.

To leave, cancel the ACS task with PA2 (+ ignore the nasty messages). Then enter: dis amdac fast.

When checking a machine, enter the commands:

Q LOG or
Q LOG ALL for machine check logs

Q CLOG or
Q CLOG ALL for channel check logs

D_MACLOG for macrocode event log

D EVENTS for ACS event log

D MSE or
D MSE AC for memory errors

Q STAT PCM for power and cooling history

CST //log - for firstlogout + logout files indicating console errors.

580 Series Processors

Models 5890-200 and 5890-300

amdahl®

Amdahl Corporation
1250 East Arques Avenue
P.O. Box 3470
Sunnyvale, CA 94088-3470
5K 11/85 MM001229