580

VOL. I

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- 580 Fundamentals - Vol. I

Overview

580 Subsystems:
- CPU
- Storage
- Channel
- Console
- PDU

Subsystems communicate via two unidirectional buses.

5860 - UP (32 channels)
5870 - DP or AP
5880 - MP (64 channels)

Microcode lives in microstore (or control store). Some microprocessors are also under the control of nanostore (composed of nanowords). A nanoword specifies functions of the ALU.

Power

PDU - controlled either from its own panel or the MOC.
PDB - Power Distribution Box - distribution point for power cables within each frame.
UPC - Unit Power Controller: monitors & controls power within each frame.
Power Supplies - convert 408 Hz to DC.

CPU

I-Unit: instruction fetch
stream branching
interruption priorities
pipeline synchronization
calculates effective address

The I-unit MCC contains both microcode (IUMS) and nanocode (IUNS).

The pipeline occasionally interlocks for particular instructions which require more than one cycle in a phase. A release signal removes the interlock.

The timer complex and interrupt router are considered part of the I-unit functions but physically reside on the MBC.

E-Unit: implements computation. The E-unit has three microstores:

ELCS - E-unit Luck Control Store
EECSA - E-Unit Execution Control Store A
EECSB - " " " " B

F-Unit: Floating Point Unit. This is an optional feature which enhances floating point operations. When an F-unit is present, different microcode is used in the I- and E-units. The F-unit has two control stores:

FCSA - F-Unit Control Store A
FCSB - " " " B

Storage Subsystem

The CPU cannot directly access the system bus. Access is provided by the S-Unit.

The S-Unit translates virtual addresses to absolute addresses, and manages the TLB.

S-Unit components:

S-Unit (LSI)
HSB (LSI)
MSU
MSC - Main Storage Controller
DI - Data Integrity Unit

The HSB provides two buffers:
I-Buffer: 32K instruction buffer
O-Buffer: 32K operand buffer

The MSU can hold a maximum of 128 megabytes of mainstorage. Data are handled in 32 byte lines. Eight bytes (quarterline) are transferred each machine cycle together with one check byte (for single bit error correction + double bit error detection).

Data to be written to storage are collected in the Main Storage Data-In Register and moved as a full line.
Data are moved out of storage via the Main Storage Data-Out Register

The MSC manages the MSU. It resides on the MBC and handles data requests from the other system components. The MSC generates the control and timing signals for the MSU. It generates ECC bits for storage operations. Error detection and correction occurs when data are on the buffer MCCs.

The Data Integrity Unit (DI) tracks the most current copy of data when multiple copies may exist in the O-Buffer, I-Buffer, and main store.

Channel Subsystem

A 580 can hold two IOPs, each supporting 16 channels.

The System Channel Addresses (SCA) (also called the Channel Configuration Logic (CCL)) reside on the MBC.

The channel subsystem has three components:

1. Input/Output Controller (IOC) - this is implemented on the IOP. Each IOP has one IOC together with one microstore and one nanostore. Both XA and 370-mode I/O architecture is supported by a single microprogram.

2. Bus Handler (BH) - resides on the IOP.

3. Interface Handler (IH) - one IH exists for each channel and supports either a byte mux or block channel. The byte mux IH stores 32 bytes of UCW for the active device. A maximum of four byte channels may be installed. These may only be supported in IH slots 6, 7, 8, and 9.

Console Subsystem (see diagram 1-6 on page 1-51)

consists of:

A. • Console MCC (System Service Processor (SSP))

B. • System Support Frame
- System Support Microprocessor (SSMP)
- Hard Disk Interface
- Multi Device Interface
- Terminal Processor (TP) BLCs for each console
- Console Storage Unit (2 meg. for SSP)
- Interface Handler Control Unit (IHCU)

C. • Electronics Complex
- Panel
- Floppy Controller
- Disk Controller
- MOC Interface (to Multi Device Interface)

D. • Operator's Console
- CRT
- Keyboard
- Terminal Support Interface (TSI)

A. The SSP (console MCC) is a barrel slot processor with eight slots.

Slot Ø - a 370-mode processor running ACS. ACS code is loaded into the console storage unit (CSU) residing in the System Support Frame. Control logic for accessing this memory resides on the console MCC.

Slot 1 - Macrocode's Console Service Interface (CSI).

Slot 2 - Multi Device Controller. This communicates with the Multi Device Interface in the System Support Frame.

Slot 3 - the console's channel/Bus Interface Device.

Slot 4 - Timer SAM (System Activity Monitor).

Slot 5 - Console Software Assist (CSA) - implementing the OSI (Operating Service Interface) devices. This is labeled IHCU on the barrel processor diagram.

Slot 6 - Hard Disk Controller

slot 7 - Memory Bus Handler (MBH)

The Console MCC also contains:

- Bus Handler
- CSU control logic
- Working Storage (for each slot)
- Operating State Registers (OSRs)
- Console Immediate Control (CIC) Logic handling control lines to and from the stack.
- Microcode RAM
- BCS Scan Interface for loading and examining console MCC latches in console ucode.

B. System Support Frame

1. This contains the System Support Microprocessor (SSMP) running first Atlas and later BCS, and consists of:

1. Support Processor (SPCPU)
2. Support Processor Memory (SPM)
3. Support Processor Peripheral Interface (SPPI)

BCS is held on ROM on the SPCPU card.

2. Oscillator BLC holding 580 clocks.

3. Terminal Processor BLCs - one for each console (1 MOC, 3 ROCs).

4. Console Storage Unit (CSU) memory array holding 2 MB of storage for ACS executing in slot ø of the console MCC.

5. Interface Handler Control Unit (IHCU) which communicates between the SCP and the MOC oper mode.

6. Multi Device Interface (containing the modem interface and) communicating to the barrel processor through the Driver C and the MOC.

7. Hard Disk Interface communicating to the hard disk controller in the MOC.

C. Electronics Complex

This is physically part of the MOC and contains:

- the operator panel
- Floppy controller and two drives
- Hard Disk controller and disk
- MOC interface logic

D. Operator's Console

This consists simply of a CRT, keyboard, and Terminal Support Interface (TSI).

580 Bus Structure

The 580 has two unidirectional buses. Each is 8 bytes wide plus one parity byte (one quarterline).

The A-Bus is the sending bus. The console, IOPs, and CPU place messages on the bus which are then handled by the Memory Bus Controller (MBC). The B-Bus is the receiving bus. All messages on the B-Bus originate from the MBC. The CPU components must use the S-unit to place messages on the A-Bus.

Bus messages are either one, two, or five quarterlines. Examples:

1 Quarterline - a response indicating task completion.
2 Quarterlines - SIO. message from the processor to an IOP.
5 Quarterlines - transmission of data from main store to an IOP (1 quarterline header, 4 quarterlines data).

MBC functions:

- Bus Management
- Data Integrity (DI): tracking multiple copies of data.
- Rupt Router control Store (RRCS) - a microstore implementing the Interruption Router.

An MBC bypass function permits messages to be transferred directly from the A-Bus to the B-Bus.

In a DP/MP configuration a second stack adds a remote A-Bus and remote B-Bus permitting intercommunication between the stacks. See figure 1-2 in the FERM.

Scan Facility

The scan Facility is used by ACS to capture tens of thousands of latch states. I-unit error latches are display on scan page 55. Other error history scan pages are: 90, 91, 92, 93, and 94. The contents of these pages freeze upon error detection.

Data may also be scanned <u>into</u> the latches.

Scan Screen Assignment permits groups of scan pages to be assembled on a scan screen.

The same latch may appear on multiple pages under different names.

Physical Components:

Number	Description
Ø1	CSI frame
Ø2	SSF
Ø3	Channel Extension (optronal)
Ø4	PDU
Ø5 + Ø6	MOC
Ø7, Ø8, + Ø9	ROCs

CSI Components (frame Ø1)

6 Power Supplies
Power Distribution Box (PDB)
UPC
2 Fans
Stack (holding max 13 MCC)
2 Side Panels

Stack Components

The stacks can hold up to 13 MCCs. Each board is 11" x 13", and can hold up to 121 CSI chips.

The MCCs are, from the top down:

position	function
MØ3	Console MCC (System Service Processor)
MØ4	IOP1 (optional)
MØ5	IOPØ
MØ6	Hardware Measurement Interface (HMI) - optional
MØ7	MBC
MØ8	S-Unit
MØ9	Buffer MCC (odd bytes)
MIØ	Buffer MCC (even bytes)
MII	I-Unit
MI2	E-Unit
MI3	Floating Point Unit (F-Unit) - optional

The A-Bus and B-Bus are implemented in the printed circuit board side panels.

System Support Frame (frame Ø2)

Components:

- 8 Power Supplies (for Channel, MDC, & MSU)
- UPC
- PDB
- MSU (Swing Gate)
- Channel/Console/CCA Gate (Fixed Gate)
- Cable Entry Panel (for 16 channels)

The MSU will have all possible driver and terminator cards, but the number of array BLCs will depend on the quantity of memory installed and the type of BLC (a maximum of 128 MB may be installed).

Channel Extension Frame (frame Ø3)

The optional channel extension frame supplies connections for 16 additional channels. The bus and tag connectors are all that reside in the CE frame.

The additional channels require additional IH BLCs in the SSF and IOP1 in the MCC stack.

Consoles

Physical consoles consist of one Electronics complex (frame Ø5) which, together with a terminal (frame Ø6) forms the MOC.

Three additional ROCs (frames Ø7, Ø8, & Ø9) may be placed within 250 ft of the SSF.

Power Distribution System

Two types of power supplies are used:

Type 9

115 lbs.
208 VAC, 4ØØ Hz input
5.2, 5.Ø, 3.6, or 2.Ø VDC, 420 amps output

Type 1Ø

63 lbs.
2Ø8 VAC, 4ØØ Hz input
5.2, 5.Ø, 3.6, or 2.Ø VDC, 125 amps output

With both types of supplies, the filters, fans, and regulator PCBs are FRUs.

All 580 UPCs (there are two) use four BLCs and have five slots (slot 4 is empty).

slot	
Ø1	Power Supply Interface
Ø2	UPC Alarm Board
Ø3	UPC Sequencing
Ø5	Air Sensor Controller

Power Distribution Box

The PDB is the point of connection for all power cables arriving from the PDU.

Power Distribution Unit (frame Ø4)

The PDU monitors and distributes all AC power to the 580, and supplies DC power for the UPCs.

580 Dual Processor (DP)

In a 5870 DP configuration, the base system frame numbers are prefixed with 1- and the second stack is designated 2-Ø1. The second stack has fewer MCCs since it does not own channels or memory.

580 Multiprocessor (MP)

An MP is two complete 580 system closely coupled and under the control of a single SCP. The CPUID BLC in the SSF identifies the processors in the MP configuration.

- Power -

Two types of power supplies are used within the 580. They are interchangeable within type since the power supply connector has jumpers which determine the voltages to be delivered at each particular location in the 580.

Both types are capable of supplying:
+5.Ø, -5.2, -3.6, and -2.Ø VDC

Type nine delivers 420 amps.
Type 10 delivers 125 amps.

The signals coming from the power supplies may be interrogated at the UPC. FERM p. 6-15 has a chart listing the signals and their locations on the UPC jacks for each supply in the SSF.

In addition the type 9 and 10 supplies, four specral power supplies are used. They are:

1	PDU	PS2	24V	EPO
2.	Electronics Complex	PS1	+24, +5, -5, +12, -12	
3.		PS2	+5	logic gate, Maint panel
4.	Operator Console	PS1	+5, -12, +12	TSI card, keyboard ...

The power supply id (PS2, for example) references the sequence in which they power up as well as a physical location designation. Slave supplies power up to a preset voltage and current level, and then a master powers up to supply the necessary current for a bus to reach a specified voltage. The output of the master is variable and depends on the needs of the bus.

PS 5 in the CSI frame was originally a slave to PS6. This has proved unnecessary and therefore dropped from later 580s. PS6 was subsequently renamed PS5.
If the CSI frame has 6 supplies, it is an old style (+ PS5 is a slave to 6). If the frame has only 5 supplies, it is a new style.

All power supplies in the SSF are masters.

When more than one supply is attached to a bus, each must be "balanced" to deliver the appropriate voltage. To change a supply:
- make physical connections
- adjust the voltage
- adjust the balance (for slaves only).

The power supply PCB has only two pots: voltage and balance.

Each supply has four FRUs:
- PCB
- Two fans
- Air filter

For a thermal check, examine the fans and air filter. For a power check, re-adjust the voltage and balance. If this does not work, swap the PCB with another supply.

Bus output voltage is measured where it is used rather than at the supplies. FERM p. 6-20 lists power tabs on the CSI stack. The best place to measure voltage is at the capacitors. These are described in the FERM.

PDB

There are two PDBs in a 580. Input consists of on cable each for:

- UPC Logic
- -5.2 VDC for UPC Power
- 50/60 Hz
- and 4 cables for 415 Hz.

There are two ground systems:

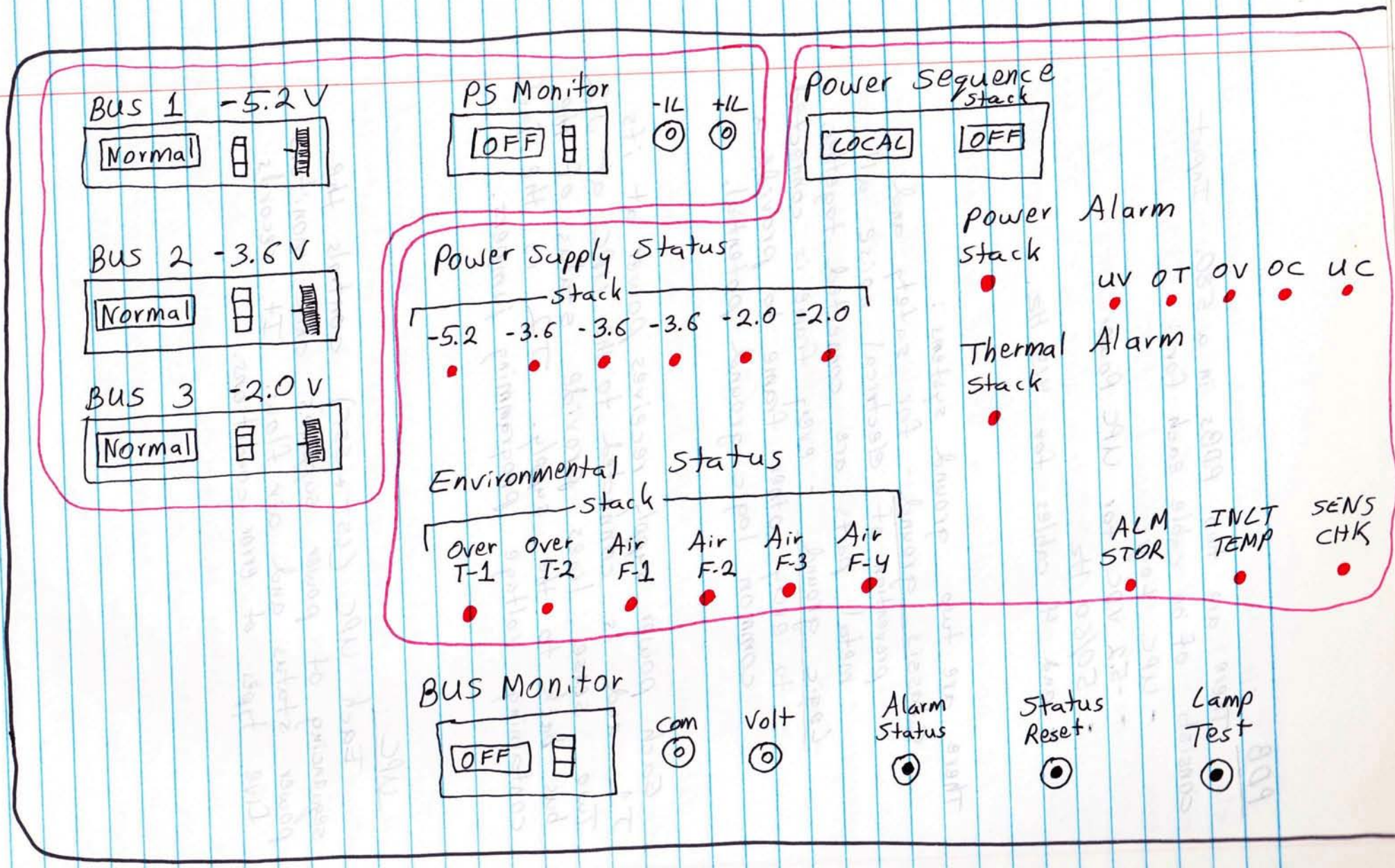
- Chassis ground - for safety and prevention of electrical noise all metal parts are connected together.
- Logic ground - every frame is connected to every other frame to provide a common logic ground potential.

Each power supply receives power at its J1 and is connected to the UPC at J2. Two sense lines provide status of the bus back to the supply. J2 is the jack containing voltage programming jumpers.

UPC

Each UPC (LSI-SSF) controls the sequencing of power supplies and monitors power status and air flow. It records five types of error conditions.

LSI UPC


Bus 1 -5.2 V
Normal
Bus 2 -3.6 V
Normal
Bus 3 -2.0 V
Normal
PS Monitor
OFF
-IL
+IL
Power Sequence
stack
LOCAL
OFF
Power Supply Status
stack
-5.2
-3.6
-3.6
-3.6
-2.0
-2.0
Power Alarm
stack
UV
OT
OV
OC
UC
Thermal Alarm
stack
Environmental Status
stack
Over T-1
Over T-2
Air F-1
Air F-2
Air F-3
Air F-4
ALM STOR
INCT TEMP
SENS CHK
Bus Monitor
OFF
com
Volt
Alarm Status
Status Reset
Lamp Test

UPC Controls

Power Sequence - Local/Remote thumb-wheel and PS1 - PS6 (or 5) sequence switch.

Power Alarm - indicates where the alarm was generated. The LSI UPC only has the stack.

UV, OT, OV, OC, UC - indicates the specific type of alarm condition. This indicates the type of error, and the Power supply status lights will indicate the supply generating the error.

Power Supply Status - has a LED for each supply. On means okay. Off is error.

Thermal Alarm - indicates that an OT condition has occurred. System shuts down when this comes on.

Environmental Status - indicates the exact sensor detecting the problem. See FERM p. 6-5 for LSI frame sensor locations, and p. 6-7 for SSF locations. Functions as a warning unless Thermal Alarm is also on

ACM STOR - turns on when an alarm occurs and remains on until reset. If this is on, press the Alarm Status button to see the alarm stored.

INLT TEMP - incoming air is too warm.

SENS CHK - indicates broken or disconnected sensor.

Bus Monitor - selects the power bus to be sampled at the adjacent terminals. These permit voltage measurements.

Status Reset - Pressing this button together with Alarm Status will clear a stored alarm.

PS Monitor - this thumb-wheel selects one of the power buses for sampling at the adjacent terminals. This permits current measurement.

Buses - Each bus switch has a thumb-wheel for Normal / Margin selection, plus a wheel to vary the amount of voltage margin. Read FEB 58ØØØ83 before performing margins.

Power sequencing - when the UPC is set to remote, the PDU will send a PWR PIK signal causing each supply to be sequenced on, in numerical order, with 150ms delay between supplies. If problems occur, the UPC sends a PWR CHK back to the PDU and stop sequencing. If no problems occur, the PWR COMP is sent. Upon receiving this signal, the PDU will raise PWR HLD and drop PWR PIK.

Power down is initiated by the PDU removing the PWR HLD. The supplies are sequenced off in reverse order with 150ms separation.

For an alarm condition, power is sequenced of in reverse order with .5ms separation. If the UPC is in LOCAL mode, the alarm condition is only displayed and not transmitted to the PDU.

Each UPC has four BLCs. These are functionally displayed on FERM p. 6-1.

Sensors - there are two types: temperature only, and temperature and airflow. These are detailed in the FERM on p. 6-4.
Two mechanical switch airflow sensors, A4 and A5, have been disabled per FCO 122325.

Power Distribution Unit (PDU)

The PDU contains three power supplies:

* Two type 10 supplies (PS1 + PS3) located at the very bottom of the panel holding the control panel. They supply -5.2 to PDU logic and UPCs.
* One special supply for +24VDC EPO power. PS 2 can function off of 50/60 Hz or 400 Hz. It has a CB for each input source. Also, LEDs indicate which source is connected. These provide a quick way to determine if either power source is not available to the PDU.

Only one of the CBs should remain on during normal operation. With both CBs on, the potential for a ground loop exists.

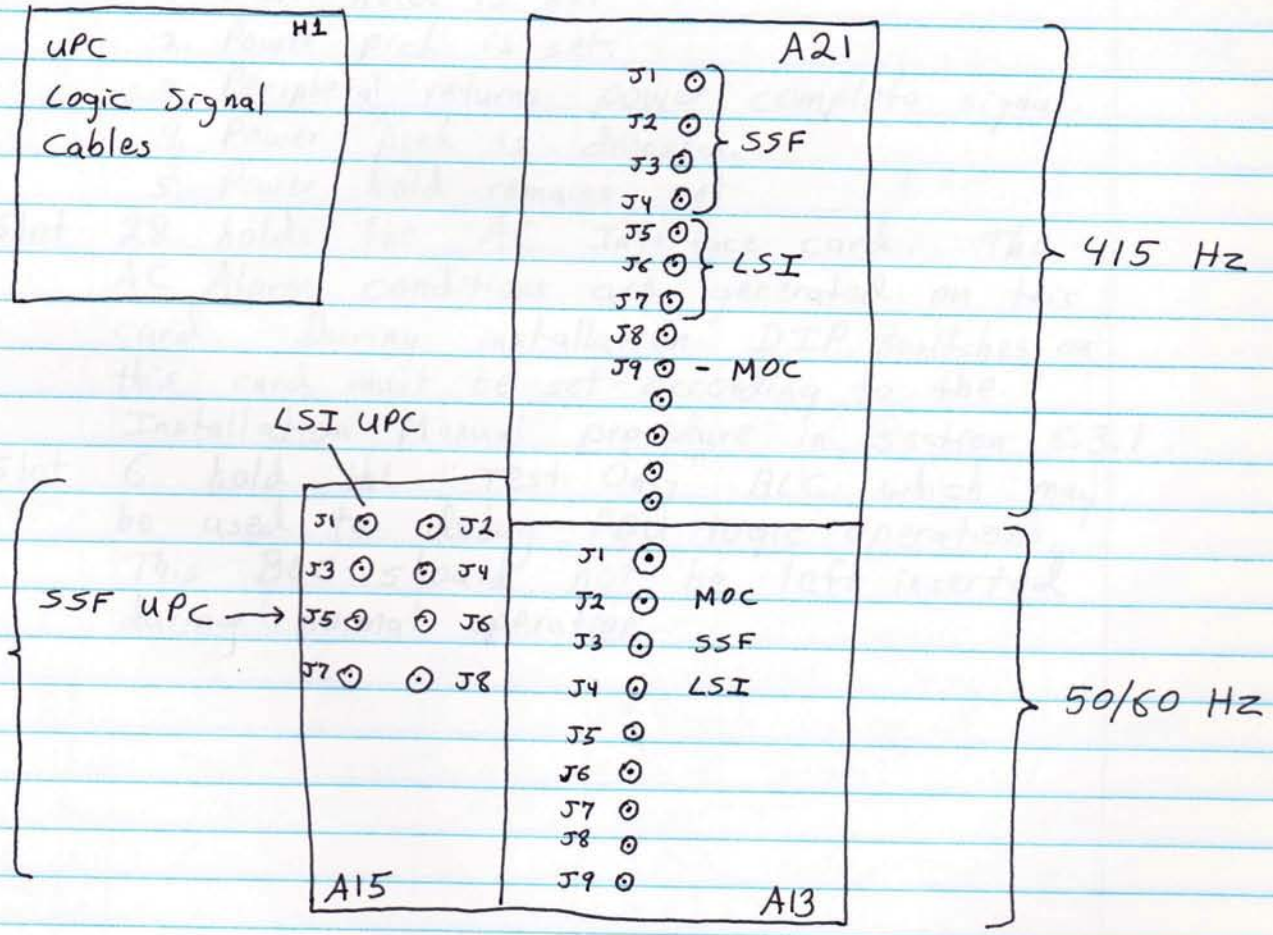
The +24 VDC energizes the EPO contactors in the AC Sequence Controller and is therefore known as the EPO supply.

AC Alarm - located beneath PS2 (EPO supply), this functions even with PDU logic power off (from PS 1). This indicates MG Abnormal, UPS Warning, MG Frequency, MG Alarm, and Undervoltage.

AC Sequence Controller - located beneath PS2 next to the AC Alarm. This manages AC sequencing to prevent the sudden application of a large load. The relays are held with +24 VDC. When all relays close, an AC Complete signal is sent to PDU logic. During power down, the contactor for the cooling fans is held for 5 minutes longer than the others.

50/60 Hz Transformer - at the bottom of the panel holding PS2, the 50/60 Hz transformer converts incoming AC for use of the fans. Permissible input is 208, 220, 230, 385, or 415 VAC. Output may be either 220 or 230 VAC. Voltage combinations are selected by taps and must be selected and verified at installation.

Contactor Center contains the cables going from the PDU to the 580 supplies. Panel A21 distributes 415 Hz; panel A13 distributes 50/60 Hz; and panel A15 distributes -5.2 VDC to the UPCs (from PDU PS3).

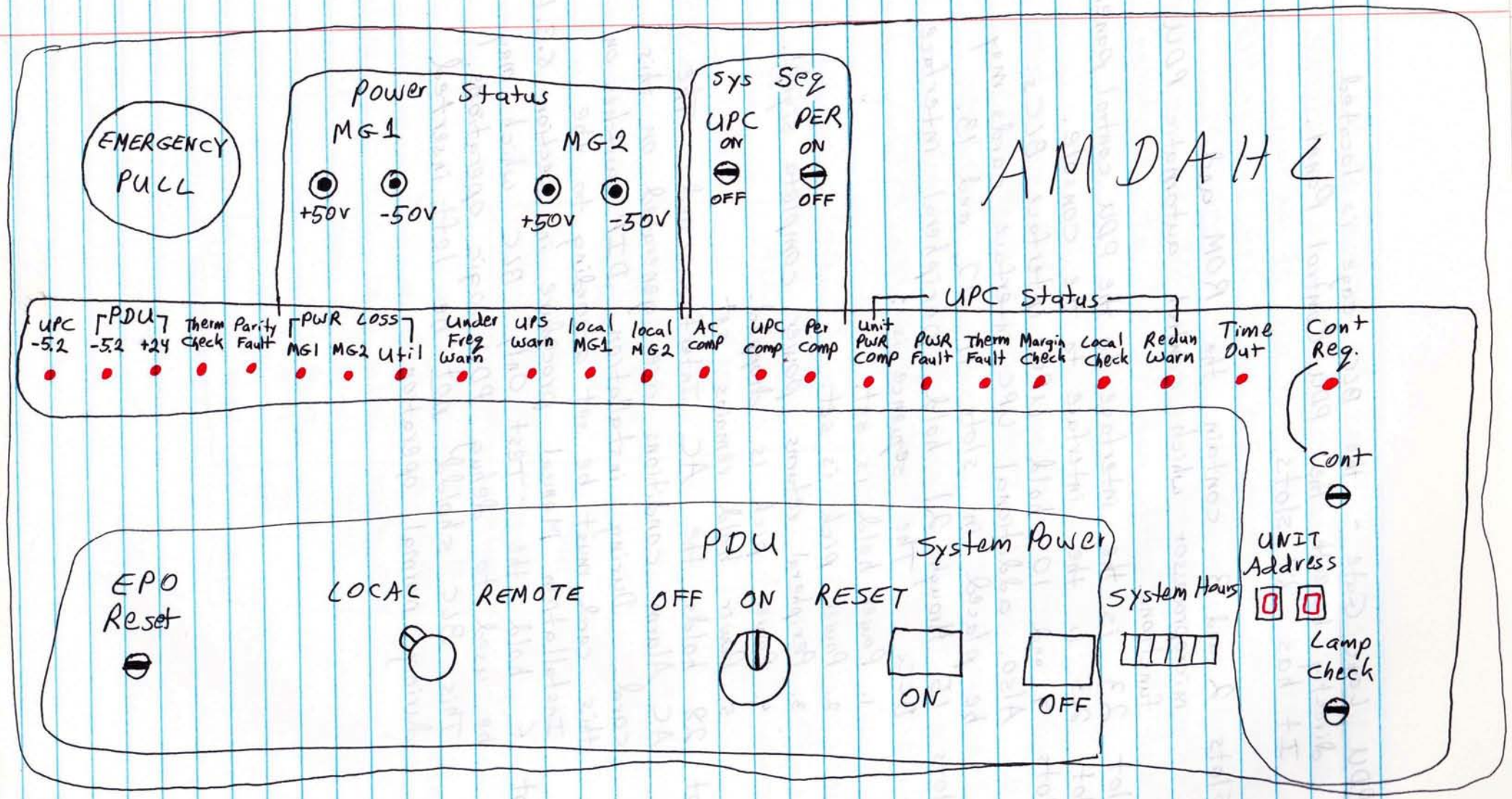


PDU Logic Gate - the BLC cage is located directly beneath the PDU Control Panel. It has 28 slots.

Slots 2 and 3 contain the ROM and microprocessor which control automatic PDU functions.
Slot 23 is the interface to the PDU control panel.
Slot 25 is the interface to the console.
Slots 9 and 10 hold UPC interface BLCs. Also, additional UPC interface cards may be placed in slots 11, 12, and 13.
Slots 15 through 21 hold peripheral interface BLCs. The sequence is:

1. Power hold is set.
2. Power pick is set.
3. Peripheral returns power complete signal.
4. Power pick is dropped.
5. Power hold remains set

Slot 28 holds the AC Interface card. The AC Alarm conditions are generated on this card. During installatron DIP switches on this card must be set according to the Installatron Manual procedure in section 6.3.1.
Slot 6 hold the "Test Only" BLC which may be used to debug PDU logic operations. This BLC should <u>not</u> be left inserted during normal operation.


EMERGENCY PULL
Power Status
MG1
MG2
+50V
-50V
+50V
-50V
Sys Seq
UPC
PER
ON
ON
OFF
OFF
AMDAHL
UPC Status
UPC -5.2
PDU -5.2
PDU +24
Therm Check
Parity Fault
PWR Loss MG1
PWR Loss MG2
PWR Loss Util
Under Freq Warn
UPS Warn
local MG1
local MG2
AC comp
UPC comp
Per comp
Unit PWR comp
PWR Fault
Therm Fault
Margin Check
Local Check
Redun Warn
Time Out
Cont Req.
Cont
EPO Reset
LOCAL
REMOTE
PDU
OFF
ON
RESET
System Power
ON
OFF
System Hours
UNIT Address
Lamp Check

PDU Control Panel

Sys Seq -

UPC ON/OFF - when ON, includes UPCs in the power-up sequence (for UPCs switched REMOTE).

PER ON/OFF - when ON, includes Peripherals in the power-up sequence (if they are controlled via the PDU).

UPC -5.2 V - When on, -5.2 VDC is available to the UPCs.

PDU -5.2 V - When on, -5.2 VDC is available to the PDU.

+24 V - When on, +24 VDC is not available. Either PS2 is off or EPO has been pulled.

Therm Check - PDU thermal problem has occured.

Parity Fault - PDU μprocessor error.

PWR LOSS

MG 1 - } 415 Hz voltage dropped below minimum
MG 2 - }

Util - Voltage has dropped; phase lost, or fan CB tripped.

Under Freq Warn - indicates problem w/ 415 Hz.

UPS Warn - UPS power is about to be lost. This is usually a signal from a solid state converter.

Local MG1 - MG voltage is being sensed at the source rather than at the PDU.

Local MG2 - same

AC COMP - All AC contactors have closed.

UPC COMP - UPC power-on sequence is complete (or UPCs have been manually bypassed).

Per Comp - Power-on sequence complete for all peripherals controlled through the PDU.

UPC Status - 7 lights report status of UPC in Unit Address:

Unit PWR COMP - DC power completed normally.

PWR Fault - UPC has lost DC power due to OC, OV, or UV.

Therm Fault - UPC has detected thermal check.

Margin Check - UPC has a power supply in margins.

Local Check - UPC is in LOCAL mode.

Redun Warn - UC detected on 580 UPC.

Time Out - PDU logic is waiting on a UPC. After an interval, CONT REQ will light.

CONT REQ - Automatic sequencing has stopped and manual intervention is required to allow the PDU to continue.

Atlas

Atlas is an 8085 machine language program resident in a PROM on the SPCPU BCC (02-A2-B1-07) in the SSF. The SPCPU is the only card required to execute Atlas.

The function of Atlas is to verify that the hardware required by BCS is operational. It validates the SPM (where BCS will be loaded), the Floppy Disk Controller (FDC), and communicates to the console CRT and the Maintenance panel ECD. The path to the CRT (of MOC or ROC) goes through the appropriate Terminal Processor BCC.

Atlas requires RAM for working storage. This is also contained on the SPCPU and, together with the ROM, is referred to as the shadow memory.

BCS requires 80K of storage. Unfortunately, Atlas's 8085 processor can only address 64K. In order to load the upper 16K of SPM, Atlas employs bank switching. Port F8 on the 8085 determines which of two 16K banks will be addressible as C000 to FFFF at a given instant. These are banks 3 and 4. If F8 is set to 1, bank 4 is accessed. When F8 is 0, bank 3 is used.

The bits in port F8 are potentially confusing. In the micro world, the bits are numbered in reverse order from System 360. Thus, the controlling bit (ALT BANK SEL) is numbered bit 3 but is bit 4 in IBM terminology.

FERM table 5-15 list the 8085 ports assigned to components of the SSMP; FERM table 5-19 lists the bits of port F8.

System Panel - selected controls:

Interrupt Switch - presents an external interrupt to macrocode.

IMPL Switch - resets and loads Atlas, BCS, ACS, microcode, + macrocode. This is the white button.

Maintenance Panel - selected controls:

Power On - with PDU in REMOTE, this causes the power-up sequence to begin. In a two PDU MP system, the secondary system should be powered up first.

Console IMPL switch - with the FE key off, reloads BCS and ACS. With the FE key on, only BCS is loaded.

Floppy Select - selects which drive to use in loading BCS.

PDU seq - a power-up or down sequence is in progress.

Error Code - signals status from the SSMP.

SUP PROC RESET - resets SSMP and restarts Atlas in debugger mode

Atlas has three functions:

1. Test the environment for BCS and load BCS.
2. Provide control for floppy-based diagnostics (some of these are executed automatically prior to the load of BCS).
3. Provide a debugger.

To meet these functions, Atlas has three parts:

1. boot program
2. monitor
3. debugger

Atlas and BCS both communicate with a single maintenance terminal. This terminal is selected by the Display Station membrane switch. Atlas ordinarily displays only in case of error.

The Atlas Rolling Byte Monitor (RBM) permits communication of errors through the two-digit ECD during boot sequence.

- Boot Error Codes -

10	System Status Register
11	System Control Register
12	SSMP Data Bus
13	TP Control Register
14	TP Data Bus Register
15	Shadow RAM

Once an error code is displayed, additional codes may be viewed by pressing any Display Station switch. Error codes 10 through 14 are followed by two additional bytes of information. Error 15 is followed by four additional bytes. Pressing the Display Station switch repeatedly causes the RBM to repeat the series of bytes.

Boot Sequence

1. Determine the reason for restart by checking port 8.
2. Test the Terminal Processor BCC in the SSF. The TP card may be tested at any time by pressing ALT and TEST/PF25. This validates the path between the TP BCC in the SSF and the TSI BCC in the MOC.
3. Test the timer and PIC - if errors are encountered here, a message will be written to the CRT and Atlas continues! Pay attention. If BCS comes up, a faulty SPCPU card may be difficult to diagnose.
4. Check the floppy drives.
5. Load and executes floppy-based diagnostics:

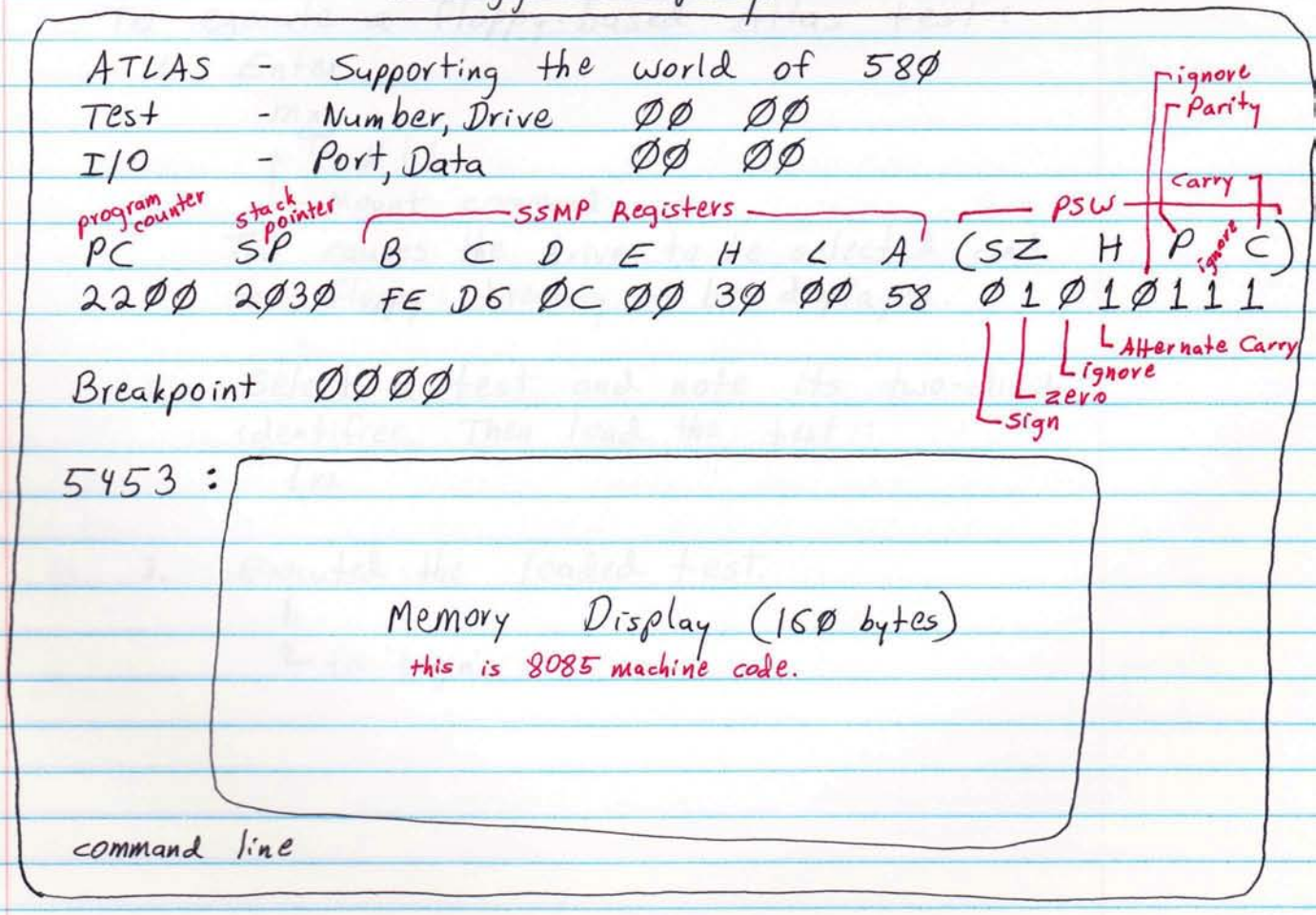
A1Ø1Ø - SPM memory test. This does not test the forth bank. To do that, manually switch banks.
A1Ø2Ø - Port test
A1Ø3Ø - SPCPU scan path test.

6. Finally, BCS is loaded & started.

Atlas error messages and ECD codes are documented in the FE/SE User's Guide on page 5-17. This table associates a FRU with each error. Atlas messages to the CRT appear only if a maintenance terminal has been selected. Atlas discontinues ECD once the TP/CRT path has been validated.

When Atlas encounters an error, it enters either Monitor or Debugger modes. Atlas commands are only a single character followed, when necessary, by operands. Monitor and Debugger commands may be entered without regard to the current mode since Atlas automatically switches if appropriate.

Debugger Display



The contents of the program counter, stack pointer, and any register may be altered with the 'x' command:

```
x r nn[nn]
  |  |  |
  |  |  └ data. PC and SP are two-byte regs.
  |  |
  |  └ Register mnemonic
  |     P = PC (Program Counter or instruction address)
  |     S = SP
  |     B, C, D, E, H, L, or A
  |     F = Flags
  |
  └ x command
```

A complete explanation of Atlas commands may be found beginning on page 5-6 in the FE/SE User's Guide.

To execute a floppy-based Atlas test:

1. Enter

   ```
   m xx
   |  |
   |  └ Ø | 1
   |
   └ Mount command
   ```

   This causes the drive to be selected and the floppy directory to be displayed.

2. Select a test and note its two-digit identifier. Then load the test:

   ```
   l xx
   ```

3. Executed the loaded test.

   ```
   b
   ↑ for 'begin'
   ```

The Atlas monitor screen lists flag bits which control a test. These flags may be altered after a test is loaded with the command:

zfs

where z is the alter command

f = a - all flags
c - cycle section
d - diagnose on error
f - force error display
h - halt on error
i - identify test
l - loop on error
m - manual mode
n - loop the nugget
s - stop before nugget
u - unconditional loop

s = 1 - on
Ø - off

Monitor commands may <u>not</u> be issued prior to loading a test. If this happens, Atlas will crash and must be restarted by pressing SUP PROC RESET.

All Atlas commands are lower case with one exception. The command 'U' This command passes control to the location where BCS starts. If BCS is not resident, the SSMP crashes.

- BCS -

Functions of the Basic Control System:

1. Reset the console MCC
2. Load console control stores
   - odd/even microcode
   - nanocode
3. IPL ACS
4. Troubleshoot the SSP
   - scan out console MCC latches & registers
   - alter console memory, registers, PSW, & microcode
   - execute Field Diagnostic Tests (FDTs).
5. Act as a floppy disk controller for the SSP.

BCS software lives on a resident floppy (in drive Ø) which is loaded by Atlas, and a non-resident floppy (drive 1) which hold scan pages. The console MCC microcode and nanocode reside on the BCS resident floppy. Updates to the console MCC code are made with a BCS patch command.

The progress of the BCS load from floppy is reported in the ECD.

ECD Displays	
1A, 1B, 1C	- Atlas is running
4Ø	- Boot pgm brings in BCS loader
4Ø, 41 ... 63	- Count of BCS tracks loaded
ØØ	- success
F2	- Unexpected EOF (bad floppy)
F4	- BCS not on floppy
FD	- Timeout (Floppy unit down)
FE	- Floppy I/O error.
CØ	- Checksum error; probable SPM error.

See FE/SE User's Guide page 8-4 for a more complete list of codes.

BCS, like Atlas, is written in 8085 machine code. Since Atlas occupies 6K of PROM, and BCS lives in the SPM, it is possible to switch back & forth between the two systems.

BCS performs tests on:
- Maintenance Panel
- Hard Disk & Hard Disk Controller
- Console Storage Unit (where ACS will live)
- Multi-Device Interface
- System Clocks
- Cables

Atlas loads BCS in response to three actions:
1. System Panel IMPL (white button)
2. Maintenance Panel Power-On
3. Console IMPL

The 580 uses a clock of 23 nanoseconds from an oscillator of 43.5 MHz. BCS is able to margin the cycle time by using one of two alternate clocks.

BCS files are peculiar.
- They cannot be created, destroyed, or increased in size.
- Files may be renamed
- Each file has an attribute byte
- Files may be copied.
- File names, sizes, and attributes may be displayed with the command: LST L Ø/1

Barrel Processor

The console MCC uses an 8 stage interleaved barrel slot processor with 8 slots. The eight stages are:

1	2	3	4	5	6	7	8
Fetch PC	Fetch Instrn	Decode Instrn	Get A	Get B	Load Addr	Adder Cycle	Write Results

Each of the slots is in each phase of the pipe for one cycle. There is not a need for interlocking.

Each slot executes a microprogram from control storage. Control storage is not modifiable. Each slot has its own 128 byte (00-3F) working storage area in MCC RAM.

Slots communicate through a 512 byte commonly addressible area known as the mailbox. This consists of 256 two-byte fields which are detailed on FERM p. 5-14.

Slots

Slot Ø - A 370-mode processor is emulated by Console MCC microcode. This slot processes the ACS instructions which actually reside in the Console Storage Unit (CSU).

slot 1 - CSI - handles communication with the CRT when in SYS mode (macrocode)

Slot 2 - Multi-Device Controller: communicates with the floppy drives, modem, CRT, and printer.

Slot 3 - Channel - this slot acts as a channel for ACS I/O operations. It actually processes the SIO.

Slot 4 - Timer and systems Activity Monitor - this is the console timer, not the system timer.

Slot 5 - Interface Handler Control Unit: this program acts as an IBM 3274 to communicate with the CRT in operator mode. The CRT is a 3277 device.

Slot 6 - Hard Disk Interface. This program is dedicated to disk I/O and is faster than slot 2 for disk I/O.

Slot 7 - Bus Handler. This functions as the console MCC's interface to the two system buses.

An example:
ACS will issue a SIO for the hard disk. The channel will be notified via mailbox and then decode the SIO. slot 3 notifies slot 6 via mailbox. The I/O will be performed, with the data moving into or out of CSU. When complete, slot 6 notifies slot 3 which notifies slot Ø.

Control store, working storage, and mailbox all reside in MCC RAM. When not working, each slot runs an idle loop that simply checks mailbox repeatedly for service requests from the other slots.

BCS corrects console MCC MWPEs by determining the address of the failing address and scanning the correct code into the RAM from the microcode file on floppy. Changes to Console microcode are contained in HWS and the field is notified via a TIB. The BCS PAtch command is used to apply the patch.

Troubleshooting

Floppy - ECD codes 18-1E identify floppy problems (also check CRT messages). If the error is detected with BCS go back to AHas for problem determination.

Terminal - ECD codes 05-07 identify terminal display errors. The TP BLC displays an "Amdahl" logo in the absence of software.

Maintenance Panel - if the MP fails, the 580 may still be power-up from the PDU with no additional intervention.

SPM - ECD codes 03, 04, 2A, 2D, C1, & C2.

Scan - Scanning involves both the SPPI BLC and a chip on the Console MCC.

Clock Control - clock control and margin selection is actually performed by BCS even when it may be initiated by ACS commands. Suspect the SPCPU, SPPI, console MCC, and system oscillator BLC.

The Pre-reqs vol. 1, beginning with page 4-42 contain detailed path explanations for the following functions:

ACS Hard Disk Path (Disk address is Ø2)
BCS Scan (see Scan Screen 5, pages 8 & 9)
ACS Floppy Path (floppy address is Ø3)
ACS Modem path
ACS Bus Path
ACS Terminal Path (for all modes: MAINT, SYS, & OPER)
ACS CSI Path (macrocode to the console)
ACS OSI Path (console OPER mode)
This path utilizes Bus & Tag connectors in the SSF cable entry to link the IHCU to a channel.

Advanced Control System (ACS)

ACS is loaded from the console hard disk into CSU and executes on slot Ø of the console MCC.

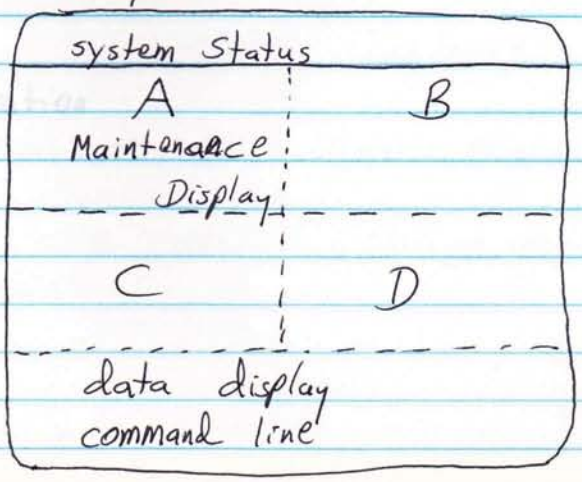
Functions:

1. load microcode
2. load macrocode
3. Reset
4. Handles mch & chan checks
5. Scans latches
6. Diagnostics
7. Supplies configuration info
8. Monitors resource utilization
9. Emulates I/O devices
10. Supports AMDAC
11. Handles error recovery

ACS keys

Test Req - retrieves the last commands
PA1 - clears command line
Alt/PF24 - restart the keyboard handler
Cancel - stops the current command
start/stop - starts & stops the processor(s)
PF keys - have recommended standard settings. see HWS.

ACS display



The maintenance display area has four quadrants to which output may be directed by appending Qx to most any command.

The lower data display area is for small amounts of data such as a PSW.

ACS Commands - 3 categories:

A - FE key & Master console
B - Master console
C - any display station

Multiple ACS commands may be entered at one time by separating each command with a slash (/).

Online help is available by entering a question mark (?) or a command followed by a question mark.

Command types:

Alter / Display
Query / Set
Enable / Disable
File System
Scan
System Modification
SAM
AMDAC
CONFiguration
Install
Misc.

Some Display commands:

D G - system GPRs
D SR - System Regs
D UG - user GPRs
D CR - control regs
D PSW - current PSW (on line 22)

Enable/Disable alters various features of ACS, such as:

ENABLE AUTOVERIFY

which permits the effects of a command to be seen on the screen without having to re-display the effected storage or register.

Console Diagnostic Monitor (CDM) is a background process of ACS that handles diagnostic execution. CDM status is presented on user screen 4 (D U4). CDM is started with DIAG and ended with ENDDIAG.

Test are labeled with a alphabetic character followed by four numeric digits. A test consists of:

Test
Test Group
Test Case
Test Instance

They reside on the Diag minidisk or on floppies.

Test are executed through the steps:

Initialize
Load
Begin

or I/L/B

Specific test or subsets may be specified. CDM is documented in Chapter 18 of the FE/SE User's Guide.

ACS File Commands

File commands manipulate files on the hard and floppy disks. The hard disk is organized into minidisks, each functionally specific. Each floppy drive is also handled as a minidisk.

ACS Minidisks

(blank)	- Root ACS directory
alt	- Alternate ACS directory. This would become the root if the primary fails.
drive0	- Floppy drive 0
drive1	- " " 1
page	- scan page formats
uc	- microcode
log	- MCH & CHN check logs; ACS event log.
mlevel	- machine level database
user	- customer working area
cprocs	- cprocs
mccsave	- hardware configuration files
bups	- help files
sys	- macrocode
diag	- diagnostics
xadata	- IOCDS files
dump	- main storage dumps
sysdata	- more macrocode.

The alt minidisk contains a back-up of ACS and may be accessed via the BCS command:

IPL D PARM A

This loads the alternate copy of ACS and the ALT minidisk becomes the root directory.

Each minidisk (including the floppies) can contain both files and sub-directories. To use a floppy, issue the ATTACH command and then treat it as any other minidisk. Afterwards, issue a DETach.

To access files, a path must be specified. Each directory is preceded by a bar (|):

|directory|sub-directory|file name

Absence of a bar restricts the search to the current directory.

Q Disk permits displaying the status of all minidisks. A FREE operand causes the amount of free space for each minidisk to be displayed.

The LST command displays the contents of a directory. LST has long (L) and sorted (S) options to govern the display. The Long display lists the timestamp and other information. LST with no directory name lists the files on the current directory.

By default the current directory with the FE key off is |user. With the FE key on, it is |CPROCs.

PWD - print working directory returns the name of the current directory. The FE key must be on to use this command.

CD - change directory

Common File Commands

CP - copies files
CPT - copies all files in a named directory
MV - movefile (functions as a rename).
CMP - compare
CD - change directory.

ACS Scan

ACS supervises recording and setting of 580 latches. A latch is a logical holding point for a signal. During a reset, ACS sets all latches to an appropriate state.

Information taken from a scan-in is formatted into scan pages. The formatting is based on information in the PAGE minidisk. FERM section 1.3 contains an index of all scan pages grouped by functional unit. The Scan Page Reference Manual contains explanations of every field on every page.

Latches may be examined with display commands:

D PA # quad

D PA 65 QC ← display scan page 65 on screen quadrant C.

ACS groups related pages together into scan screens. Each screen holds 4 pages. There are 64 scan screens.

D S#

or

PA1 + PF#

↑ where # = scan screen number.

Scan Screen Assignment (SSA) is the grouping of pages into screens. This assignment may be modified by explicitly displaying a page while a screen is displayed.

D S1/D PA 65 QD

Thereafter (until ACS is IPLed) scan page 65 will appear in quadrant D of scan screen 1. To make this change permanent, issue:

SAVE SSA

To revert to the ACS defaults, issue:

RST SSA

Ordinarily, the SSA is <u>not</u> changed via the SAVE command.

<u>Scan Redisplay</u> - Enabling scan redisplay causes ACS to refresh the scan screen approximately once each second with status from a running machine. If this is desired, issue

EN RDP SCAN

ACS is unduly burdened by redisplay, so avoid using it.

The default state is for redisplay to be off. The command

DIS RDP SCAN

accomplishes this task.

During a machine check, ACS records the state of all latches into an error log. To examine a specific log, issue:

EN LOG# 01

01 ← 0 or 1 for CPU on an MP when in UP mode.

LOG number

Once the ENable command has been issued, the display page and screen commands will act on the log file. When done, enter:

DIS LOG

Special Functions:

SCANIN - this command has two functions. It permits modification of any latch, and lists the physical latch address. To accomplish the former, once SCANIN is in effect, change the contents of a field and press ENTER. To list the location, alter the value of the field and press PF12.

FAST - this is a dedicated ACS function to quickly display scan pages on a stopped machine.

ACS Editor - ACS has a full-screen editor which is documented in chapter 17 of the FE/SE User's Guide. Invoked with ED.

Primary Commands - entered on the command line:

Copy
DELete
FILE
Insert
[LINE] - make the line number entered the top line
Left
Move
Pf - set a PF key
Quit
Right
SAVE
Search - any set of characters may serve as delimiters
To - move the cursor to named row & column.

All primary commands must be entered in lower case. Abbreviations consist of the letters capitalized above.

Line Commands

xi	- insert
xd	- delete
dd	- block delete
c	- copy line
t	- to here
cc	- block copy
m	- move line
mm	- block move
r	- repeat line
rr	- block repeat
.	- make this the current line

Aroid using multiple copy and move commands.

CPROCS - CPROCs consist of a series of ACS commands plus arithmatic and logical operators.

To create or change a CPROC file, use the EDitor. CPROCs live on the /user mini-disk.
To delete a file, use the remove command (RM).

Variables: Must be declared.
Integer - 4 bytes
Character - variable
Arguments - parameters entered when invoking the CPROC. May be either Int or char. These may not be assigned a value within the CPROC.
S# - number of argument variables assigned. $Ø through $2Ø. $Ø is the name of the CPROC.
$STAT - return code from the last ACS function.

All variable names must begin with $ and may not exceed 14 characters.
One dimensional arrays are supported. When an array name appears as an operand with use of a subscript, all elements in the array are used as operands. This is useful when altering or storing GPRs, for example.

String Manipulators
len - length
substr - substring
cat - concatenate

Constants

strings - text enclosed in double quotes.
binary - # sign. 10011#
decimal - . 756.
hex - nothing or x C0Fx

CPROCs are completely described in chapter 16 of the FE/SE User Guide.

Error Logs

Machine Checks - a maximum of 10 machine check logs may be stored (0-9). Each has a time stamp. When the maximum is reached, the oldest is over-laid.

Q LOG - lists the most recent log.

Q LOG ALL - the most recent is flagged w/*.

LOGK - forces ACS to write a log. This would be used after a checkstop.

PROT LOG# - protects a log from being over-laid.

UNPROT LOG# - unprotects

ENABLE LOG# 0|1 - selects a stored log for viewing.

DISable LOG# - cease viewing selected log.

Channel Check Logs - 100 channel check logs may be stored. When the maximum is reached, the most recent log is repeatedly over-laid (number 99).

Q CLOG - display timestamp of most recent log.

Q CLOG ALL -

D CLOG # - displays contents of selected log.

External Damage Logs - recoverable checks cause an abbreviated log to be written. This consists of scan pages 90 to 95. Nine of these logs may exist and can be printed with AMDEREP.

Q ELOG - most recent
D ELOG# - displays contents

Macrocode Event Log - macrocode errors are logged in the file |SYS|EVENT.LOG. When this gets too full, logging ceases. To clear:

RM "|sys|EVENT.LOG"

quotation marks are necessary because the filename is capitalized.

Reset Commands

The various reset commands cause ACS to perform a series of steps initializing parts of the 580 to predetermined conditions.

The reset commands have three useful operands:

P - print (to screen) each reset step.
L - list the reset steps without actually performing the reset.
V - verify the reset by listing it to the screen and then waiting one second before executing it. The reset may be aborted by pressing the PA2 key.

Resets

RS PO - Reset Power-On: this is the highest level reset. It does everything. This takes approximately 3 minutes and executes 73 steps.

RS CONF - Reset Configuration: this does not load microcode and does not clear the TOD clock. It may be used to supply new configuration informatron for a 370-mode system.

RS CONF must NOT be used to re-initialize XA configurations.

RS SYS - Reset System: this command resets the 580 without changing the GPRs or memory. The Clear option will cause memory & registers to be cleared. RS SYS should be used after implementing a new IOCDS.

RS IO - Reset I/O: this causes the IOPs to be reset without effecting the rest of the 580, and may be useful in diagnostic situations.

ACS Load Commands

IMPC - manually loads all microcode.
LMP - may be used to load microcode into individual units of the processor.
IML - reloads macrocode. This command may be used with the Clear option (IML C) to perform a RS SYS and reinitialize macrocode when implementing a new IOCDS.
LDMEM - this command causes a disk file (usually a diagnostic) to be loaded into 580 mainstore. For example:

LDMEM -d Ø |user|dirt

will load dirt into domain Ø storage.

RDMEM - this command copies 580 mainstore to an ACS disk file.

Clocks - Each of the three 580 clocks (free, gated, I-unit) may be controlled. However, the gated clock is the one most frequently manipulated.
CL OFF - stops the gated clock
CL - advances the clock one machine cycle.
CL xx - advances the clock hex 'xx' cycles.

SET RATE Instructron - this causes the CPU to perform enough cycles to execute one instruction and then stop.

SET RATE PROCESS - returns the 580 to normal process mode.

Margins - this adjwts the 580 clock control.
F - fast
S - slow
N - normal

XOP - permits an opcode to be inserted directly into the pipe.

SAM - System Activity Monitor - SAM does not generate a lot of overhead for ACS and therefore may be left running. Use of SAM is described in chapter 20 of the FE/SE User's Guide.

ACS Status Display - the four-line status display at the top of the screen may be selectively enabled and disabled:
EN RDP STAT - enable
DIS RDP STAT - disable

ACS Maintenance

Disk Dump and Restore (DDR) - this is a utility loaded from BCS which runs in place of ACS. It is used to create the ACS files.

Prior to using DDR, the disk must be formatted with the Hard Disk Diagnostic, A826Ø. The BCS LOAD command initiates this.

DDR is loaded using the BCS IPL command. It is used to:

- Configure & initialize minidisks
- Copy minidisks
- Make backups

DDR may only be used with DDR format files. It may not be used against ACS files.

For the Minidisks which are installed via DDR, the procedure is:

Configure (followed by PF1 and PF3)
Restore minidisk-name

Once ACS is placed on disk, other minidisk files will be created using ACS commands. These minidisk areas must first be Initialized by DDR, however. ACS will INSTALL or COPY files into the areas INITIACIZED by DDR.

Once ACS is installed and patched, use DDR to make a backup.

ACS Install - the four ACS INSTALL commands permit the system to be updated and preserves back-out information.

Prior to issuing an install, the floppy drive containing the update must be ATTACHed to ACS.

INSTALL Filename - copies a file from floppy to the hard disk.

INSTALL LIST listname - accesse a file containing a series of install commands to be executed plus any ACS commands required.

Whenever a file is updated, ACS Install processing renames an unmodified version by appending an alpha O to the filename. This identifies an Old file.

Install UNDO - this is used for backing out a change. The Old files on the specified minidisk are re-activated by removing the O from the filename.

Install Cleanup - this command deletes all Old files and should only be used when an update has been tested and verified (like immediately prior to adding the next maintenance).

ACS Patch - Patches are usually small changes to firmware. Microcode, macrocode, and ACS can be patched. Patches are obtained from HWS, patch floppies, or via file transfer. Patches are installed with the PATCH command.

An update is a major change to firmware. It involves an entire replacement of a file and is performed with the INSTALC command.

Patches are usually applied from floppy using INSTALC CIST with a filename of ALC. This file contains the actual PATCH commands.

When a patch must be manually entered (from HWS) the file is usually placed in the ICPROCS minidisk.

Patch verifies that the change can be applied (by checking 'old' values, like VER) before altering a file. The verify may be performed without making the change by using the Verify operand. A patch may be removed by using the Reverse operand.

PATCH targetfile H displays a complete patch history of a file.
PATCH targetfile S lists a summary of each patch.
Both commands generate a file called PATCH_AUDIT.

Machine Level Files - the /mlevel minidisk contains a machine level control file listing the part number and revision level of every MCC, IH, & CCA in the 580, plus the microcode levels. This file is used by ACS to determine what microcode to load. If the /mlevel file is not correct, the machine may not reset. Also, ACS uses the part numbers to distinguish between byte and block channels.

The QMC command reads the control file and permits full-screen updates. The same information in ACS memory may be simultaneously updated with the QMC ALL MEM command.

ACS Configuration Commands (CONF)

In order to reset and run the 580 hardware must be configured (in this order):

IOPs
Memory
CCAs
SCAs to IOPs
Control Units and Data Streaming Devices (370 only)
OSI
CSI

As the CONF commands are issued, ACS updates both a disk file and its copy in memory. To make the changes take effect, issue:

RS SYS

For convenience, the CONF commands are placed in a CPROC.

CONF IOP# ON - IOPs must be configured on before they may be used.

CONF MI# xx yy - Each memory increment must be configured with its addressing range.

Q CONF SYS - displays MI settings as well as other system-level specifications such as system registers.

CONF CCA# ON - an installed CCA must be configured on before use.

370-mode I/O Configuration

CONF SCAzz IOPxy MODE 370
- zz = hex SCA number
- x = IOP number
- y = hex slot number

CONF SCAzz IOPxy aa rr MODE 370 - This command configures shared subchannels.
- aa = highest unshared address. Shared subchannels begin with the next address. 8F would indicate sharing begins at 90.
- rr = subchannels will be grouped in this hex increment (10 for 16 addresses).

CONF SCA# CU# xx yy - for channels with SIOF queueing, the devices must be assigned to a CU.
- xx = beginning device address
- yy = number of devices in hex.

CONF DSD SCAxx CUy - data streaming devices must be identified

XA-mode I/O Configuration

Configuration of an XA system is far easier than a 370 system since most of the information is contained in the IOCDS. Only the CHPIDs must be related to slots:

CONF SCAxx IOPab MODE XA

xx = SCA number
a = IOP
b = slot

CONF IOCDS#

= 0 or 1 and indicates which IOCDS to use.

Q CONF IO - this command permits all I/O assignments to be displayed.

Operator Service Interface (OSI)

The 580 console is used by the SCP through an OSI assignment.

CONF OSI xx 4 - indicates a starting address and range for OSI definitions.

SET OSI xx 3277 DS1 - assigns one of the OSI addresses as a 3277. (Another should be set as a 2540).

An internal cable attaches the console to one of the byte channels. Then, when an I/O is directed to the defined address, the IHCU intercepts it and routes it to the console.

A RS SYS C must be issued between the CONF OSI and the SET OSI.

Console Service Interface (CSI)

CSI is configured to permit macrocode to find the console.

```
CONF  SCA7E  CSI
```

Specific installation instructions will identify the SCA to be used.

SAVECONF - this command creates separate configuration files for systems that will run both XA and 370-mode at different times.

```
SAVECONF  370   - for 370 mode only
SAVECONF  XA    - for XA mode only
SAVECONF  CONF1 -
                  } for MDF
SAVECONF  CONF2 -
```

These files are then used as operands to the CONVERT command when switching from one architectural mode to another.

Note: SAVECONF and CONVERT are not needed unless the machine will be switching architectural modes.

Detailed instructions on configuring the 580 are found in chapters 9 and 10 of the FE/SE User's Guide.

CPU

Logical components of the CPU:
- I-Unit
- E-Unit
- S-Unit → Manages High-Speed Buffers

Physical components:
- I-Unit MCC (Slot 11)
- E-Unit MCC (Slot 12)
- S-Unit MCC (Slot 8)
- BUFØ MCC (Slot 10)
- BUF 1 MCC (Slot 9)

The I-Unit does not communicate directly with mainstorage. It directly utilizes the buffers and presents requests to the S-Unit.

Once the E-Unit executes, the I-unit returns results to registers or buffers.

I-Unit components:
- Register control
- Process control
- Address Generation
- I-Fetch
- Pipeline control
- Microcode

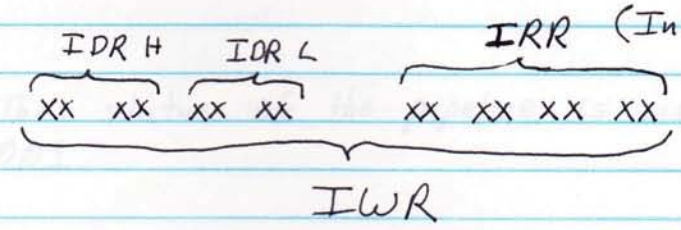
Register control - consists of
1. GPRs (use ACS command: D G)
   - User
   - System
2. FPRs
3. CRs

Process control - this is the logic which handles I-unit special processing. Normally, the instruction stream itself governs I-unit operation. Process control provides direction when an interrupt occurs (PSW swaps) or an instruction must be retried. Process control references the PSW mask bits.

Address Generation is performed separately and concurrently for instructions and operands. The Effective Address Generator (EAG) consists of an Instruction Address Generator and an Operand Address Generator.

Control store is microcode routines for execution of an instruction. The actual op code is used as an index into microstore. The I-unit RAM do not have ECC. Therefore, when an error is detected, ACS will reload the effected microstore. The ACS command Q MWPE provides a log of corrected errors.

I-Fetch receives the address of an instruction from the EAG and is responsible for loading the instruction into appropriate registers. The fetched instruction is placed in the Instruction Word Register (IWR) (or Instruction Word Buffer - IWB). Other registers are IDR, Instruction Decode Register (or Input Data Register)



The contents of the IWR are visible on scan pages 52 (IDR H+L) and 161 (IWR). During processing, instructions bubble up from the IRR to the IDR.

Pipeline - The 580 pipeline has five phases of instruction overlap. The phases are:

G - Generate
B - Buffer
C - CUCK
E - Execute
W - Write

Under ideal circumstances, an instruction completes execution every machine cycle. The pipeline coordinates the activities of the I-unit, E-unit, and S-unit.

1. Generate Phase: the address of the operand is determined and the S-unit is notified that a request is soon forthcoming. The correct routine in microstore is located by using the opcode.
2. Buffer Phase: the address of the operand is passed to the S-unit (which should have it available in the HSB). E-unit microstore is accessed using the opcode. The CUCK Control Store Address Register (CCSAR) is loaded. ← using OAR
3. CUCK Phase: the Logical Unit and Checker is a part of the E-unit. Operand data is placed in the Operand Word Register (OWR).
4. Execution Phase: actual execution is conducted by the E-unit.
5. Write Phase: The I-Unit retrieves the results from the E-unit and stores into appropriate registers or HSB.

The status of the pipeline is visible on scan page 001.

→ the R1 field of the instruction.
→ the X2 or R2 field of the instruction.

	V	R	OP	NF	12	W
G	1	1	92	1FF	FE	A
B	1	1	18	218	24	42
L	1	1		25A	35	43
E	1	1		258		47
W	Ø	Ø				4Ø

Write Address: indicates where the results will go. 1st digit indicates which set of registers. 2nd digit indicates which register.

→ Nano Function: indicates the nanocode routine controlling execution. The opcode is frequently the rightmost two digits.

→ Op Code: only preserved in the G and B phases.

→ Release: this phase has completed work and can release the instruction to the next phase.

→ Valid Bit: the indicated phase is currently executing an instruction. If the valid bit is <u>not</u> on for a particular phase, then all other flags for that phase are meaningless.

Occasionally, instructions must linger in a phase for more than one cycle. This occurs if, for instance, the operand data is not yet in the HSB (Fetch Data Interlock, FDI), the E-Unit requires several cycles (like a MVCL), and common register dependencies for multiple instructions. Whenever these situations arise, the pipeline interlocks at a phase and no movement behind the interlocked phase can occur.

FERM figure 2-6 chronicals the pipeline activities and lists the interlocks possible for each phase. Scan page ØØ1 in the lower right corner lists ten possible interlocks. To see which phase caused the interlock, examine scan page 53.

Pipeline Tags: to the right of the phase status area on scan page ØØ1 are ten tag fields. A tag is a bit of additional information about the processing requirements of the instruction. An instruction which writes to a register will have the WR tag set. Similarly, an instruction which sets the condition code will have the CS tag. Not all tags are visible on scan page 1.

The tags on scan page 1 are governed by the phase validity bit.

I-Unit Trouble-Shooting: Scan pages 1, 55, and 65 are the chief sources. Also, BUGPROCS is useful.

Scan Page 65 - the lower right lists System (S) and Process (P) damage flags for each unit (IU, EU, SU, MBC). Also, the upper left lists instruction errors (GØ, G1, and IDR) as well as address generation errors.

Scan Page 55 - the lower right repeats the system & process damage indicators. Above SY DMG, it list ADDress and DATE parity errors for I-Unit Control Store (CS ERR). ACS should reload the control store in event of this error. Time Out (TOUT) is also indicate which may not be an I-Unit problem. Check the last valid instruction in the pipe. If it is I/O, then an IOP may be at fault. Another common condition is for the S-Unit never to respond to an I-Unit request for data.

Register Parity Error - the I-unit parity checks data coming into its registers. This may detect bad data generated by the E-Unit Result Register or a corruption introduced via a side panel.

E-Unit

Components:
- OWR (Operand Word Register)
- LUCK (Logical Unit and Checker)
- Execution Facility
- RR (Result Register)
- Control Stores (LCS + ECS)

The E-Unit functions during the L and E phases of the pipeline. Input occurs at the OWR. This consists of two 32 bit registers (OWRH, OWRL). Input comes from the I-Unit (from registers) or the S-Unit (from memory). OWR contents are valid during the L phase. The data placed in the OWR by the S-Unit is done so at the request of the I-Unit. The data do not pass through the I-Unit.

The contents of the OWR may be viewed on scan page 161 as the top two words under the heading WR.

During the L phase, data passes from the OWR to the LUCK. There it is parity checked. The Luck may also be updated from E-Unit internal registers. Thus, the Luck parity checks from three sources of input: I-unit, S-Unit, and E-Unit. The E-Unit updates the LUCK when processing instructions which require multiple machine cycles.

The Luck performs logical operations on data such as compare, compact, AND, OR, and move.

Data leaving the LUCK are placed in the E-Unit registers AR and BR.

CUCK functions are controlled by the CUCK Control Store (CCS). This is loaded during the B cycle.

Execution Facility - During the pipeline E phase, the E-unit performs arithmetic functions with the output being placed in the Result Register (RR). This is a doubleword register. Execution is controlled by two control stores: Control Store A and Control Store B (CSA, CSB).

The E-unit, therefore, has three microcode files: EELCS, EECSA, and EECSB. If an F-unit is installed, these files will be different.

Scan page 100 provides an overview of the E-unit. It lists:

OWRH ← OWRL
AR ← BR
RRH ← RRL

The simplest errors are those where the CUCK detects no parity error and then the RR has bad parity. This indicates that the corruption was introduced by the E-unit.

For CUCK detected errors, consider the functions of the instruction. Were operands in registers or memory?

S-Unit and HSB

HSB reduces MSU access time by holding currently active instructions and operands in fast-access storage. The S-Unit controls data movement into and out of the buffers and main storage. Other functions include TLB and data integrity.

BUF Ø holds even bytes. BUF 1 holds odd bytes. Both MCCs hold both operands and instructions. Each buffer (IF and OP) hold 32K. Each logical buffer is further divided into two set-associatives, permitting dual searches. The set-associatives are called primary and alternate but are each of equal importance.

Since the I-Unit has separate instruction and operand logic, and this division is preserved in the S-Unit, then the two fetching operations can take place asynchronously. Store operations should never occur to the IF buffer.

Data are moved into and out of buffers in 32 byte lines.

The S-Unit has its own pipeline which runs in synchrony with the I-Unit.

I-Unit	S-Unit
G	P - Priority Cycle
B	B - Buffer Cycle
C	R - Requester Cycle
E	
W	

In the P-Cycle, the S-Unit decides which request (among I-Unit, I-fetch, MSU etc) to honor. In the B-Cycle, the buffer is access. And in the R-Cycle the data are returned to the requestor. S-Unit priority levels are detailed on FERM p. 3-7.

If the data are not in the HSB then Line Missing occurs and the I-Unit waits in a Fetch Data Interlock while the S-Unit retrieves the data from the MSU.

Parity checking of the HSB data is performed by the receiving component.

Scan page 10 lists some S-Unit activities:

- B & R cycle addresses, S-Unit opCode, & valid bit
- Line Present in Buffer Flag (CP)
- Translation already performed (TCB)

The S-Unit opcodes are explained on FERM p. 3-7.

Scan page 161 lists the S-Unit ports:

0	PF (Prefetch)
1	TR (Translator)
2	DI
IF (I-Fetch)	EV (Eviction)

Together with each port is listed the address and a wait state field (WP). If a port is waiting for an MSU fetch, then a wait code of 'A' will be set for that port. S-Unit port wait states are documented on FERM p. 3-8.

Scan page 161 also lists the Primary (P) and Alternate (A) GWRs hold data being moved between the MSU and the buffer. Each register holds 8 bytes and parity errors are flagged (*).

Of the three S-Unit components, BUF0, BUF1, and S-Unit MCC, 80% of the errors occur to the S-Unit MCC. BUF0 and BUF1 are swappable, so an error with an instruction would become an operand error if swapped.

CPU Troubleshooting

The I- and E-units use control stores. In event of an error, ACS logs the error, reloads the microcode from the hard disk, and retries the instruction. The ACS command

Q MWPE

lists a count of all errors for each control store.

containing pages 195, 65, 203, + 218.

Check Scan Screen 16 first after an error, then scan screen 1. Learn all of the pages on scan screen 1. Also, know CPU scan pages 65 and 55. See BUGPROCS and FERM section 2.2. E-Unit errors are visible on scan page 110.

Diagnostics - a set of floppy-based diagnostics, called HT diagnostics, may be loaded to test individual CPU functions, like certain instructions. DIRT and ALPHA are more generalized hard disk-based diagnostics. The most common method is to run DIRT with

ENABLE CHK STOP

to preserve error latches.

CLRSW CHK ALL releases check stop.

MBC and Bus

The 580 uses two uni-directional buses. The A bus is for sending messages; the B bus is for receiving messages. The Memory Bus Controller (MBC) MCC manages bus traffic (slot 7).

Messages are placed on the A bus by:

1. Console
2. IOP
3. CPU

Messages arrive on the B bus for:

1. Console
2. IOP
3. CPU

Messages for the MSU are received and processed by the Main Storage Controller (MSC) on the MBC MCC. Other messages are moved from the A bus to the B bus via a "bypass" route.

Two OR gates, one for each bus, select which component gets control of each bus. These OR gates are physically located on the buffer MCCs. These gates also have connections for remote buses which would belong to a second CSI stack.

The buses are physically located on the sidepanels.

Each bus holds 8 bytes plus parity (72 bits). Bus messages are in multiples of 8 bytes (a quarterline) since this amount of information may be transmitted each machine cycle. Messages are either 1, 2, or 5 quarterlines in length and consist of a header plus data quarterlines. The header may contain data.

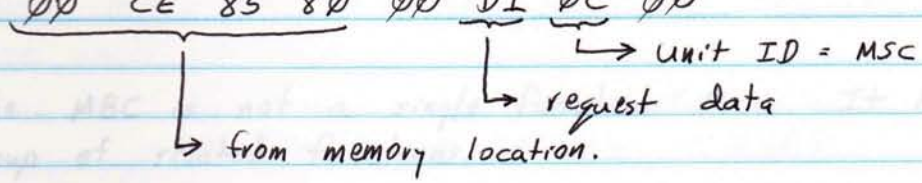
Data between the S-unit and MSU is exchanged in 5 quartline messages since a line of storge consumes 4 quarterlines (+ header = 5).

Once a message is begun, the sending unit has control of the bus until complete.

Header Message Format:

byte 5 - op code
byte 6 - A bus : destination code
B bus : source code
bytes Ø - 4 - message dependent information

All bus messages are explained in Bus Messages.
Example:



A-bus control tags:
Message Valid - causes the MBC to consider the bus values for the component raising Message valid.
Header Valid - indicates that the data currently on the bus is a header.
Bus Hold - indicates that the bus will be needed on the next machine cycle to complete a single bus message.

B-Bus control tags:
A set of Advance and Acknowledge lines exist between the MBC and each B-bus user. The MBC raises the advance line to a particular component 2 cycles prior to placing a message on the bus for that component. When the message is received, the receiver raises its Acknowledge.

A bus control tags are displayed on scan page 220 under the heading MHB.

MBC <u>subcomponents</u> grouped by function

- Bus
  - Bus Control
  - Bypass
- Memory
  - MSC (Main Storage Controller)
  - ECC
  - DI (Data Integrity)
- I/O
  - Channel Configuration Logic
- CPU
  - Timer Complex (TC)
  - Interrupt Router (IR)

The MBC is not a single function MCC. It holds a group of related functions.

<u>Timer Complex</u> - contains :

1. TOD
2. Clock Comparator
3. CPU Clock

The timer complex is described on scan pages 245 & 246.

<u>Interrupt Router</u> - routes interrupts from the IOP or Timer to the CPU based on the masks in the PSW. The Interrupt Router is the only subcomponent of the MBC utilizing microcode.

Both the Timer Complex and the 'rupt router place messages on the B bus.

Channel Configuration Logic - intercepts all messages bound for the IOPs to insure proper routing to the required IOP and channel.

Main Storage Controller (MSC) and ECC - the MSC controls the MSU.

Data Integrity (DI) - the purpose of DI is to insure that the most up-to-date copy of data is used whenever multiple copies may exist in the system (main store, IF buffer, OP buffer).

The Bus OR logic on the Buffer MCCs determine which A bus user accesses the MBC. The chosen message enter via the MBC register (called MBC Reg or MBCDR). This register feeds three units:

MBC Reg → Message Storage Registers (MSR)
MBC Reg → Bus Recorder (holds last 256 messages)
MBC Reg → Channel Configuration Table (used for I/O msgs)

The Bus Recorder is RAM which holds the last 256 A-Bus messages. These may be viewed with the ACS command:

VIEW MBC

The MSRs consist of a register for each user of the A-bus. These hold messages when the bus is busy (presumably a buffer for incoming MBC work). MSR contents may be viewed with

D MSR unitname

Unless a message is for an MBC component (like MSC) then it is directed to the B-Bus Bypass register. Thence it moves to the Buffer MCC and the B-Bus Data Register (also called B-Bus Out) and finally on to the B-Bus itself.

Non-MSU message flow:

MBC Register (MBC)
Bypass Register (BYP)
Buffer register (BUF) } on Buffer MCC
B-Bus Data Register (BBO) }
B-Bus

The contents of these registers are displayed on scan page 220 along with the control bits. The message valid control tag must be on for the contents of the register to be considered valid.

MBC Troubleshooting

Most of the traffic on the bus is data moving to and from storage. Therefore, it is highly likely that any detected error may belong to an MSU failure. Eliminate MSU errors first.

For MBC failures, use scan pages 218 and 92 together with BUGPROCS. If a bad message is being placed on the Bus, run dirt in check stop and use the ACS command VIEW MBC to capture the bad message, decode it, and determine the source.

Storage Subsystem

The storage subsystem includes the HSBs, S-Unit, MSU, and part of the MBC.

CSI: - MSC on MBC
- ECC
- DI

Non-CSI: MSU array cards in the System Support Frame (02).

The Main Storage Controller (MSC) has two functions:
1. Interfaces the MSU with the bus
2. Control the MSU (including setting and checking storage protection keys).

A storage request to the MBC arrives in the form of a real system address and is placed in the Main Storage Address Register (MSAR). The MSAR is displayed on scan page 200. Other scan pages documenting the MSC are: 203, 202, & 205. The MSC is a very reliable component.

ECC permits correction of single bit errors. ECC logic lives on the MBC and, when moving data to storage, generates the ECC byte which is stored with each 8 bytes of data. When data is moved from storage the ECC logic uses the stored ECC byte to check the data and correct it if necessary. Thereafter, the ECC byte is discarded and the data are placed on the bus with simple parity.

Data Integrity - implemented on the MBC. DI insures that the most recent copy of data is always used to satisfy storage requests. This is necessary since the IOPs and console do not access the HSB.

DI monitors the HSB and may initiate a move of changed data to storage. Also, it checks data requests of the IOPs and console to insure that the data do not reside in the HSB.

Move-in involves moving data from the MSU to the HSB. Move-out involves storing into the MSU.

Move-Out - two forms:

Short: if data in the buffer are unchanged, then the location is simply abandoned. The buffer location becomes immediately available to hold new data.

Long: Altered buffer locations are moved to their appropriate locations in the MSU.

Move-In Data Path:

	Register	Location	Scan Page, Label	r
1.	MSU array cards	MSU		ECC
2.	MSDOR (1 quarterline)	MSU	190, MS	ECC
3.	MSDR	BUF MCC	190, MSDR; 220, BUF	ECC
4.	QL Regs	BUF MCC	190, QLx	Parity
5.	OP or IF Buffer			
	or → B-Bus for IOP or Console		190, BBUS	

A Move-in always involves a full line of storage (32 bytes). However, data is moved in quarterline increments beginning with the quarterline containing the requested address.

Move-Out Data Path - a move out may be initiated by either the S-Unit or DI. It begins when the S-unit places a message on the A-bus to the MBC containing the address of the data. The MBC places the address in the MSAR (scan page 200).

The data, meanwhile, leave the buffer via the Primary or Alternate GWRs (scan page 191), to the Move-Out Data Register (MODR), still on the buffer MCC. There, buffer ECC is checked and removed and the parity bits generated. The data are then placed on the A-Bus as the four remaining quarterlines in the move-out bus message.

The MBC receives the message (having already received the address in the header) and places the data in the MBCDR. Here, ECC is generated and the data leave the MBC via the MS DIN register. All four quarterlines are then collected in the Main Store Data In Register (MSDIR) located in the MSU. Data are written to storage as a complete line.

Summary:

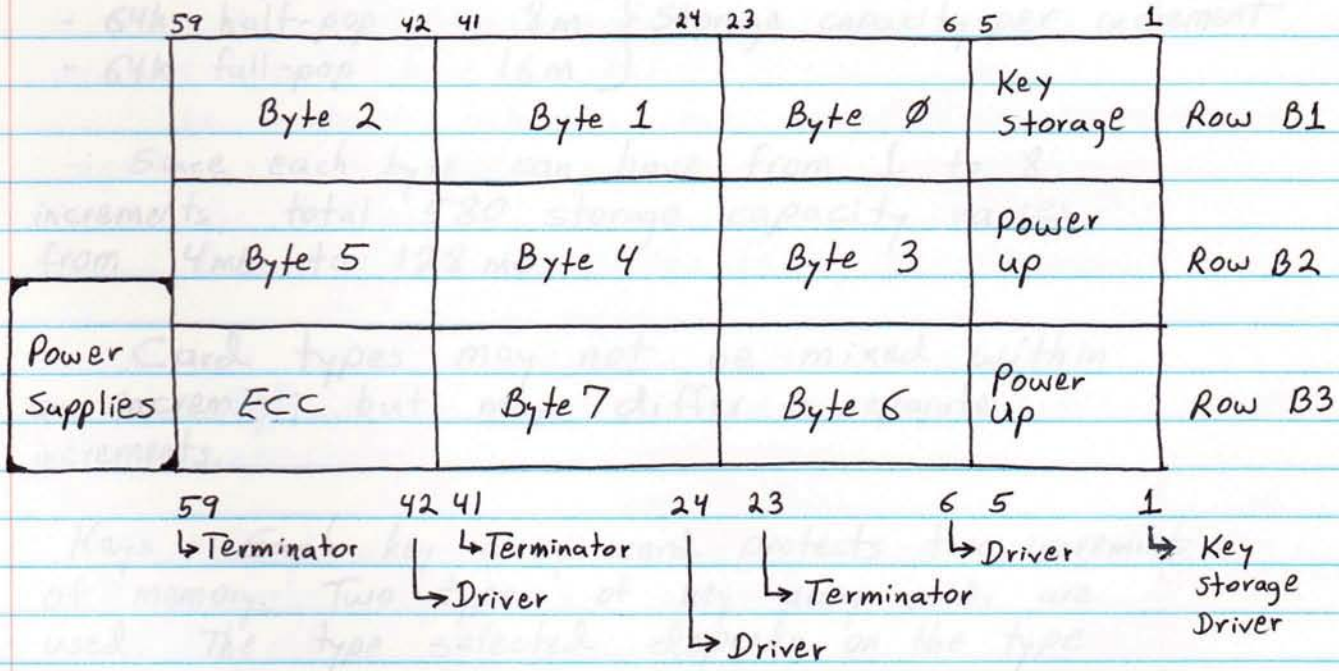
Register	Location	√	Scan Page, Label
HSB	BUF MCC	ECC	
GWR (PRI + ALT)	BUF MCC	ECC	191, PRI + ALT
MODR	BUF MCC	ECC	191, MOVOUT
A-Bus		Parity	
MBCDR	MBC MCC		220, MBC
MS DIN	MBC MCC	ECC	200, MS DIN
MSDIR	MSU	ECC	
MSU array cards	MSU	ECC	

MSU - consists of six types of BCCs:

1. Power-Up
2. Array Driver
3. Array
4. Terminator
5. Key Array Driver
6. Key Array

All control signals and data arrive at the MSU from the stack via nine red ribbon cables. The signals go first to the Power-Up cards and thence to the Driver cards. The MSDIR is physically located on Array Driver cards. The MSDOR is physically resident on the terminator cards.

Physically, the MSU is arranged with three horizontal rows, each with 59 slots.



See FERM pages 3-17 through 3-19 for listing of the cards for each slot.

Bytes Ø through 7 represent a quarterline of data plus one ECC byte. The MSU always acts on full lines of data (32 bytes).

Each byte consists of a driver card (in the low slot), a terminator card (in the high slot), and a variable number of array cards. Array cards are installed in groups of two, called an increment, and are loaded in slots from high to low. All bytes must have the same number of increments (therefore, to add one increment would involve installation of 18 BLCs). A maximum of eight increments may be installed.

The two cards in an increment split the eight bits in each byte. The card in the lower slot of the pair holds bits Ø - 3. The other card holds 4 - 7.

Memory array cards are of three types:

- 16k chip	4m	Storage capacity <u>per</u> increment
- 64k half-pop	8m	
- 64k full-pop	16m	

Since each byte can have from 1 to 8 increments, total 580 storage capacity varies from 4mb to 128 mb.

Card types may <u>not</u> be mixed within an increment, but <u>may</u> differ in separate increments.

<u>Keys</u> - Each key array card protects two increments of memory. Two types of key array cards are used. The type selected depends on the type of memory array card installed. If the increments are mixed, then the key array must be of the type to protect the larger capacity BLC.

key storage cards

Row B1, Slot	Protects Increment #
5	Ø, 1
4	2, 3
3	4, 5
2	6, 7

MSU Troubleshooting

Single bit errors may be displayed with the ACS command

D MSE A

The A operand is for Accumulated and shows all errors rather than simply the ones incurred since the last time the command was issued. D MSE A displays a matrix of each storage increment verses byte and bit.

The increment, byte, and bit may be used together with the FERM pages 3-17 through 3-19 to locate the failing BLC.

Amdahl EREP reports the failing BLC directly.

Multiple bit errors are more difficult. Eliminate any known single bit errors to reduce the probability of an uncorrectable.

Although a multi-bit error is uncorrectable, SCP processing may continue with the failing storage configured offline. This reduces the data available to solve the problem.

The first stop is scan page 65 on scan screen 16. The S-Unit (SU) will indicate Process damage. Next, scan page 195 lists the field MACH2 containing an explicit error code. See FERM p. 3-5 for a complete list of errors.

Next, examine the MCIC on scan page 203. The SE field may indicate an uncorrectable storage error if the FA0 and FA1 fields are also set to 1. Scan page 203 also has field FA indicating that the FSAR is valid.

The FSAR is visible on scan page 218. This isolates the error to an increment and byte, which implicates 16 BLCs. Positive identification is not usually possible after this point without running in check stop or astute guessing based on the QL_x registers and the hope that the hit occurred in unchanging system memory which may be displayed (using ACS D M command).

Check Stop - if the error is detected in check stop, see scan page 190 for the contents of the Quarterline registers (QL_x). One should have splats (*) by each byte. Issue the ACS command:

D MSU

to display the last line transferred out of the MSU. Compare this data with the QL buffer to reveal the failing bits.

BUGPROCS section 5.7 and chapter 6 contain information on debugging uncorrectables.

Other Errors - if an error reoccures after an array card has been replaced, fan out the driver and terminator cards. Also, remember that all nine red ribbon cables are involved in data transfers.

Be alert for numerous address exceptions in customer software. These could indicate incorrect address generation in the I-Unit or S-Unit.

Key Array Parity Error - a single key array card protects two increments. Therefore, for a key array PE, use the FSAR to identify the increment and use FERM pages 3-17 through 3-19 to locate the key card. If the problem reoccures, consider the key array driver card.

Configuring Memory - the available memory is made known to the system via the ACS configure commands:

CONF MIx aapp

where: x = Memory Increment (Ø-7)
aa = starting mega byte for the increment, in hex.
pp = indicate full or half-pop
1Ø = half-pop
11 = full-pop (used for 16k chips, as well).

The ACS command:

Q CONF SYS

displays the memory increments as configured. See ACS commands and the 580 installation manual for more details.

Warning: the MSU and the stack must both be powered down when working on either.